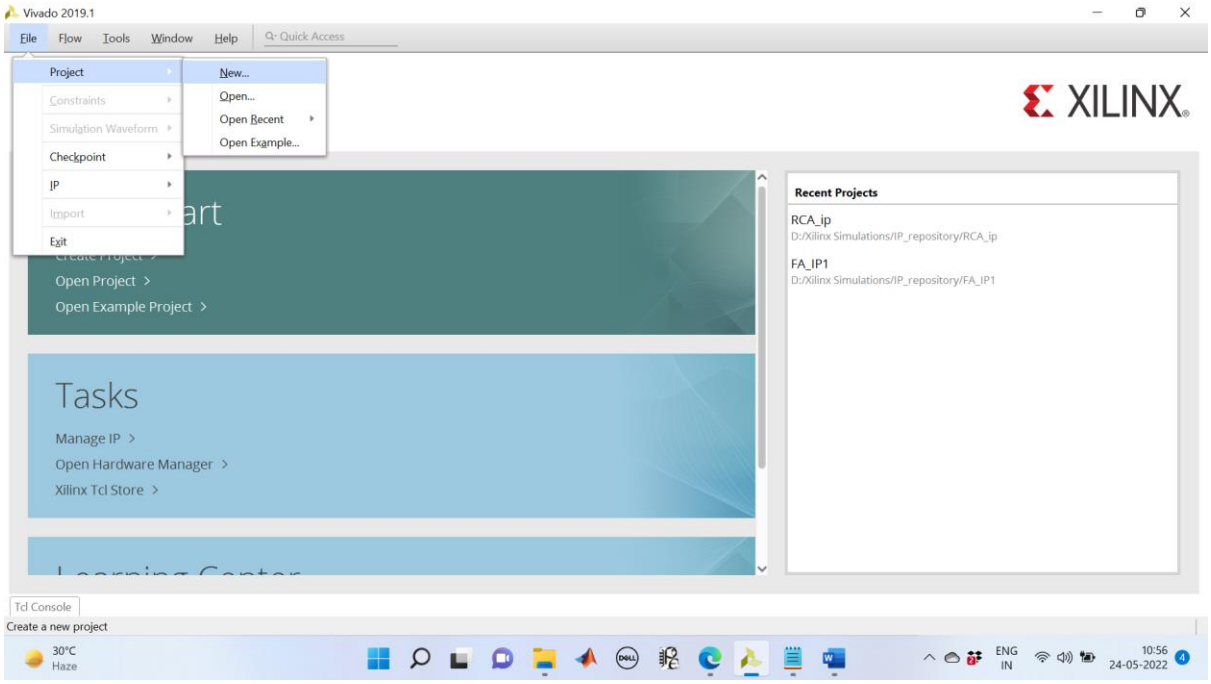
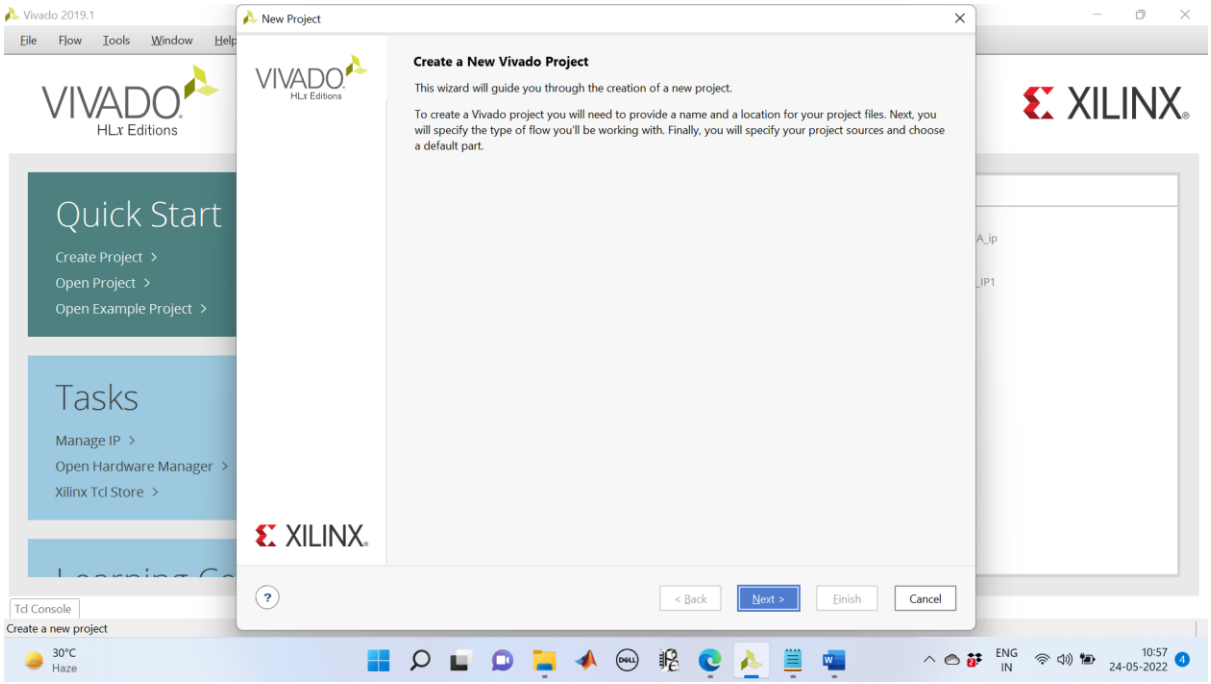
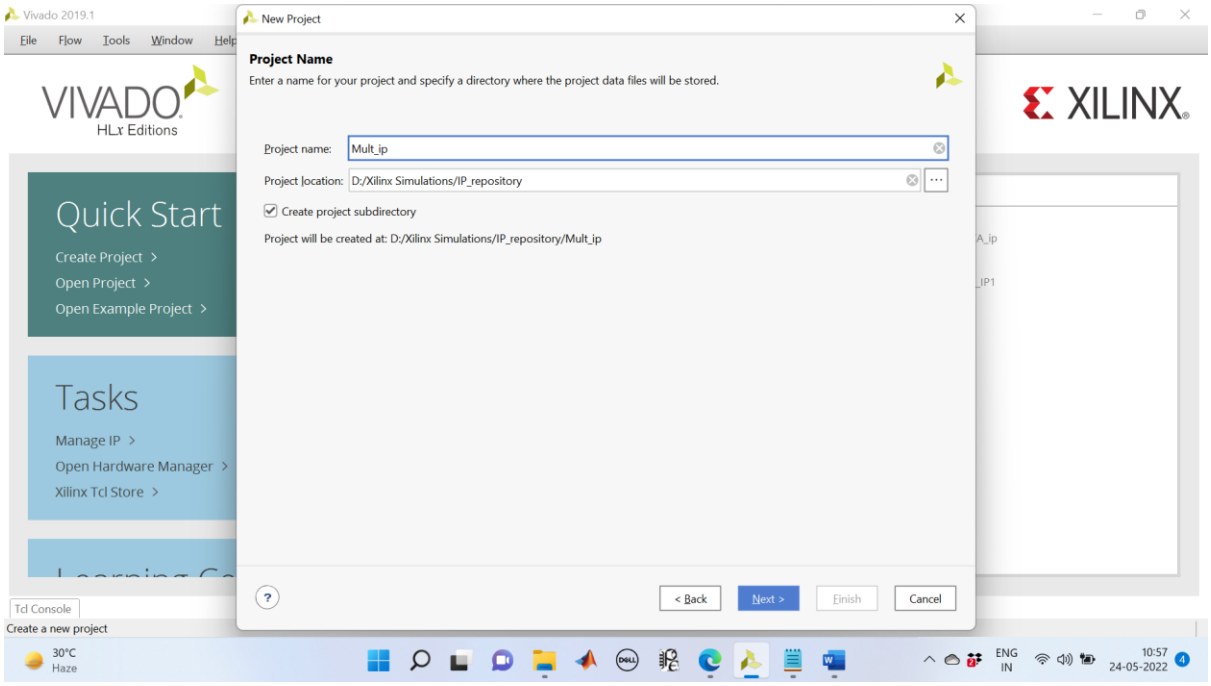
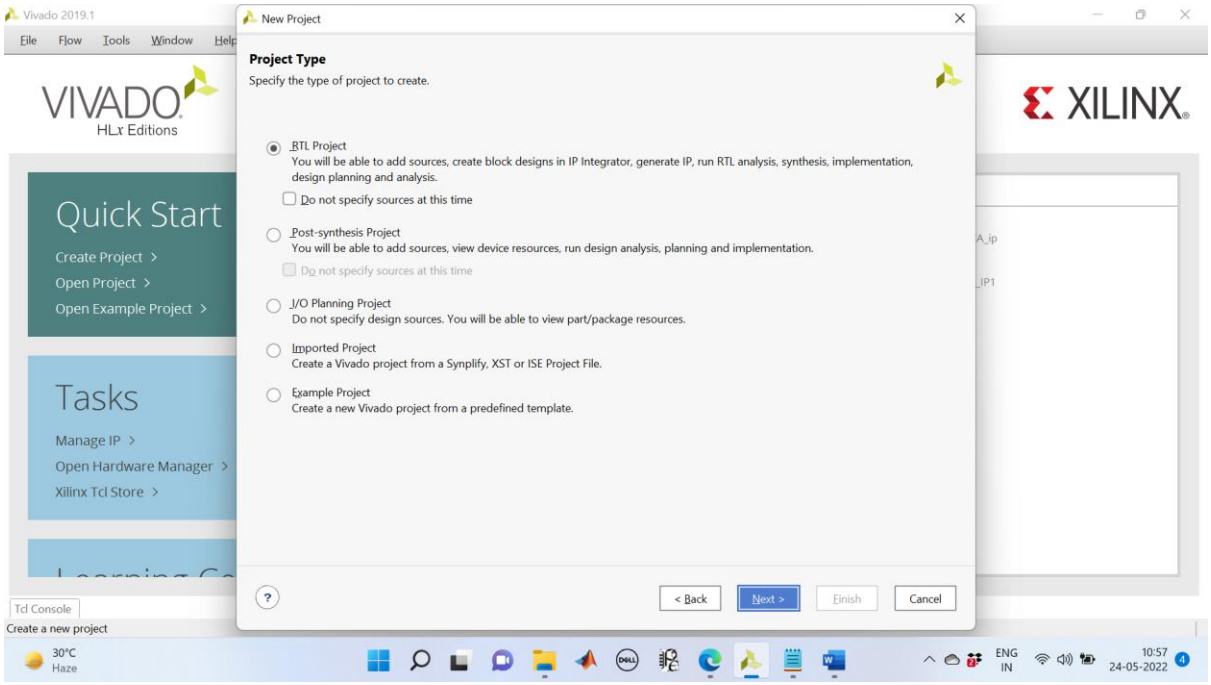
How to Create and Package an Intellectual Property






Vivado 2019.1
File Flow Tools Window Help
VIVADO HLx Editions
XILINX
Quick Start
Create Project >
Open Project >
Open Example Project >
Tasks
Manage IP >
Open Hardware Manager >
Xilinx Tcl Store >
Tcl Console
Create a new project
New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name: Mult_ip
Project location: D:/Xilinx Simulations/IP_repository
Create project subdirectory
Project will be created at: D:/Xilinx Simulations/IP_repository/Mult_ip
< Back
Next >
Finish
Cancel
30°C Haze
ENG IN
10:57 24-05-2022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XILINX
Quick Start
Create Project >
Open Project >
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Tasks
Manage IP >
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Xilinx Tcl Store >
Tcl Console
Create a new project
New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel
30°C Haze
ENG IN
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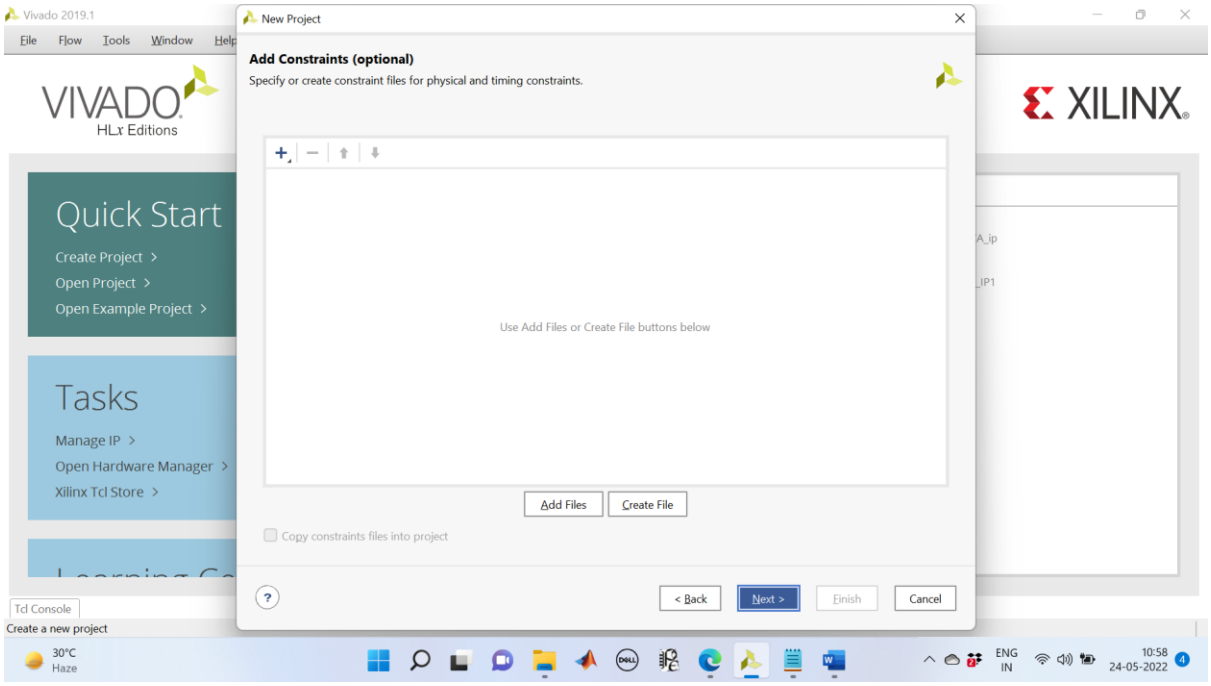
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XILINX
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Open Project
Open Example Project
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Manage IP
Open Hardware Manager
Xilinx Tcl Store
New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel
Tcl Console
Create a new project
30°C Haze
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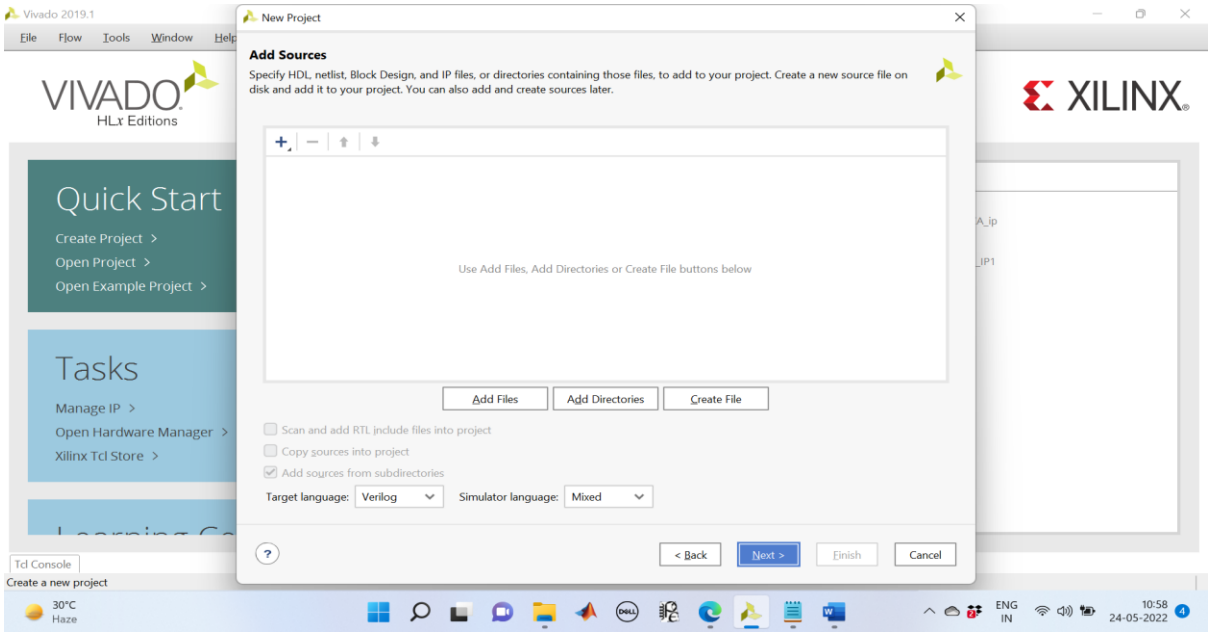
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XILINX
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: Verilog
Simulator language: Mixed
< Back
Next >
Finish
Cancel
Tcl Console
Create a new project
30°C Haze
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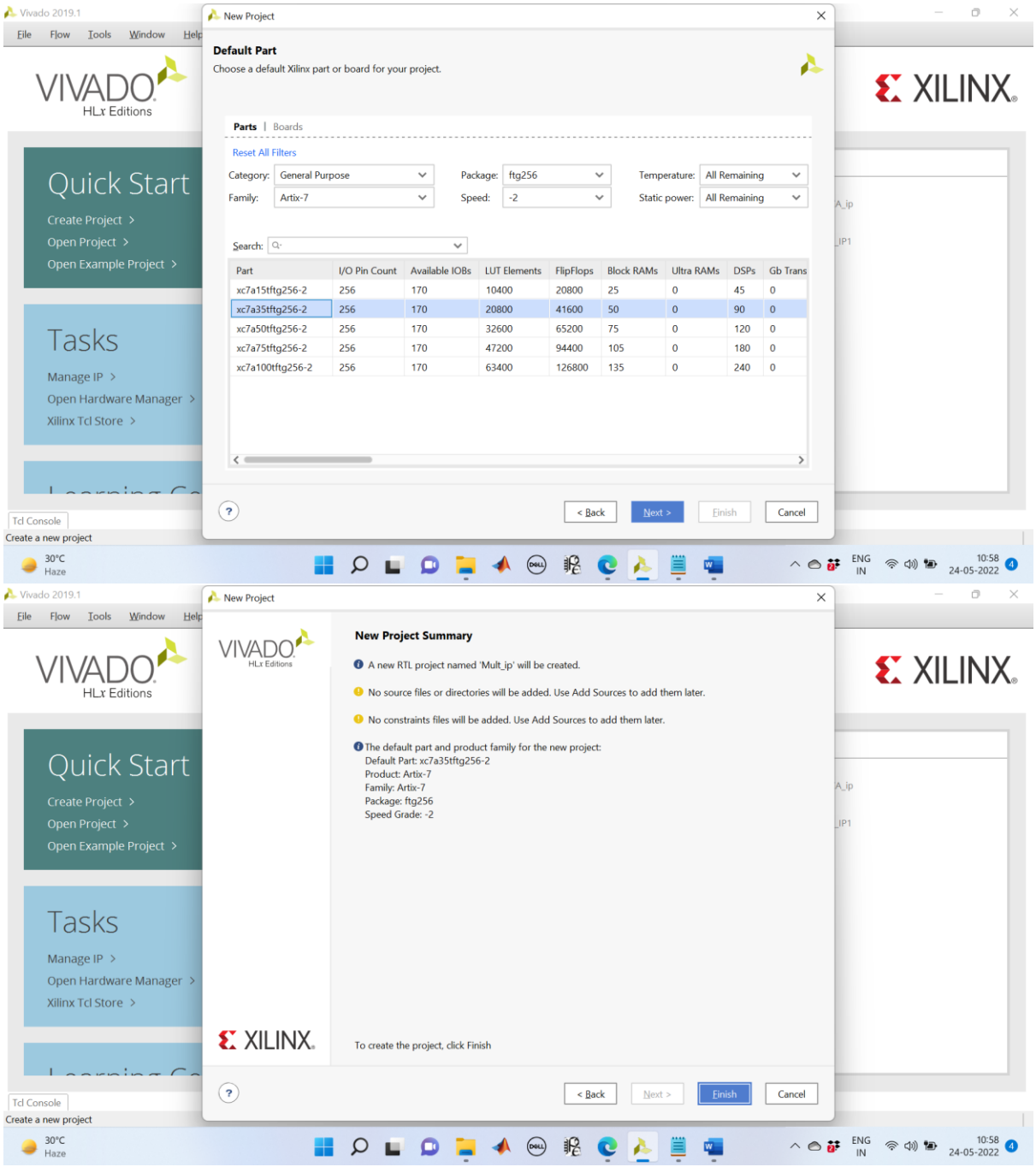
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Quick Start
Create Project >
Open Project >
Open Example Project >
Tasks
Manage IP >
Open Hardware Manager >
Xilinx Tcl Store >
Tcl Console
Create a new project
New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Category: General Purpose
Family: Artix-7
Package: ftg256
Speed: -2
Temperature: All Remaining
Static power: All Remaining
Search:
Part I/O Pin Count Available IOBs LUT Elements FlipFlops Block RAMs Ultra RAMs DSPs Gb Trans
xc7a15tftg256-2 256 170 10400 20800 25 0 45 0
xc7a35tftg256-2 256 170 20800 41600 50 0 90 0
xc7a50tftg256-2 256 170 32600 65200 75 0 120 0
xc7a75tftg256-2 256 170 47200 94400 105 0 180 0
xc7a100tftg256-2 256 170 63400 126800 135 0 240 0
< Back
Next >
Finish
Cancel
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Open Project >
Open Example Project >
Tasks
Manage IP >
Open Hardware Manager >
Xilinx Tcl Store >
Tcl Console
Create a new project
New Project
VIVADO HLx Editions
New Project Summary
A new RTL project named 'Mult_ip' will be created.
No source files or directories will be added. Use Add Sources to add them later.
No constraints files will be added. Use Add Sources to add them later.
The default part and product family for the new project:
Default Part: xc7a35tftg256-2
Product: Artix-7
Family: Artix-7
Package: ftg256
Speed Grade: -2
XILINX
To create the project, click Finish
< Back
Next >
Finish
Cancel
30°C Haze
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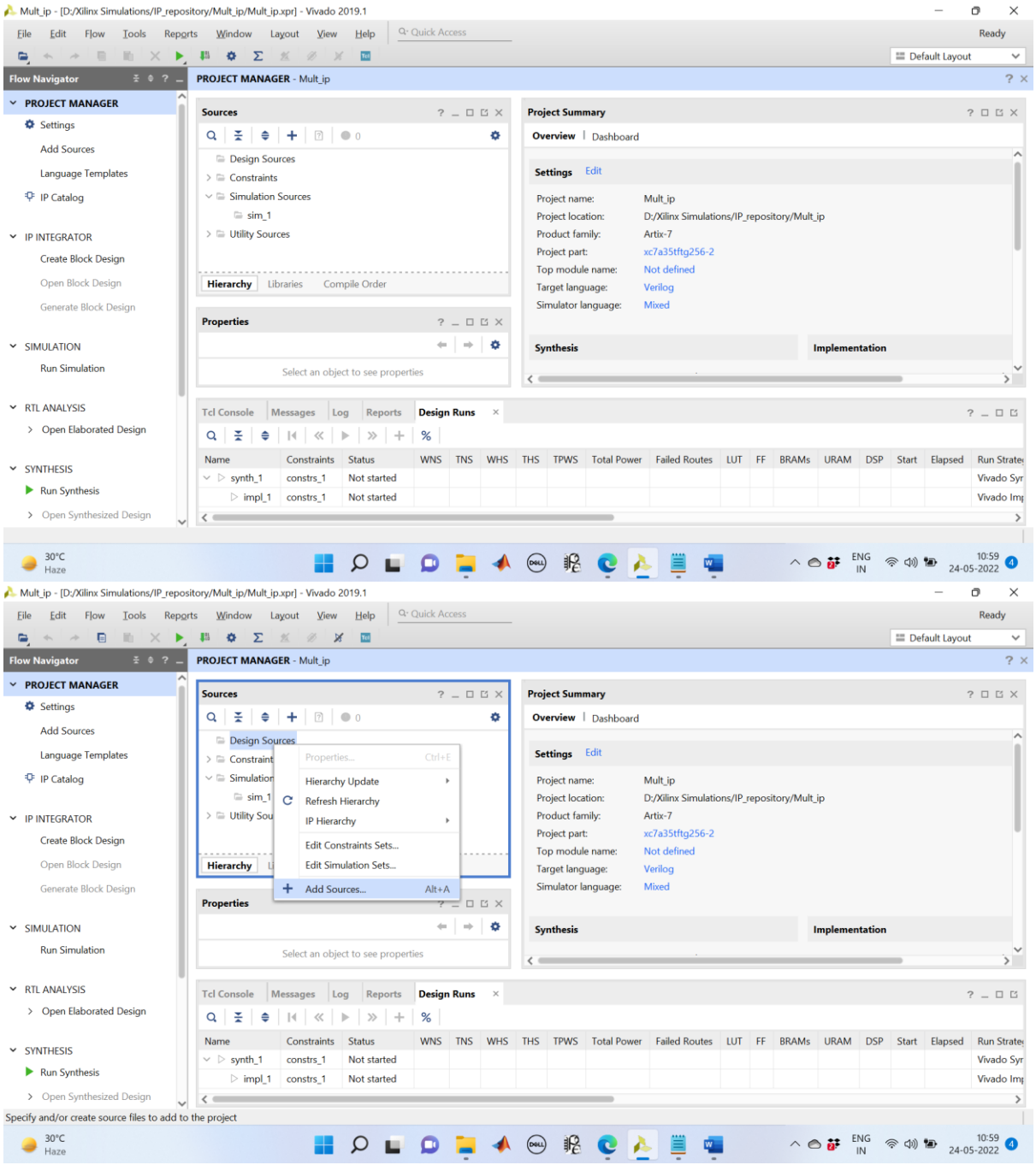
Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
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PROJECT MANAGER - Mult_ip
Sources
Design Sources
Constraints
Simulation Sources
sim_1
Utility Sources
Hierarchy Libraries Compile Order
Properties
Select an object to see properties
Project Summary
Overview Dashboard
Settings Edit
Project name: Mult_ip
Project location: D:/Xilinx Simulations/IP_repository/Mult_ip
Product family: Artix-7
Project part: xc7a35tftg256-2
Top module name: Not defined
Target language: Verilog
Simulator language: Mixed
Synthesis
Implementation
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAMs URAM DSP Start Elapsed Run Strate
synth_1 constrs_1 Not started Vivado Syr
impl_1 constrs_1 Not started Vivado Imp
30°C Haze
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Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
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SYNTHESIS
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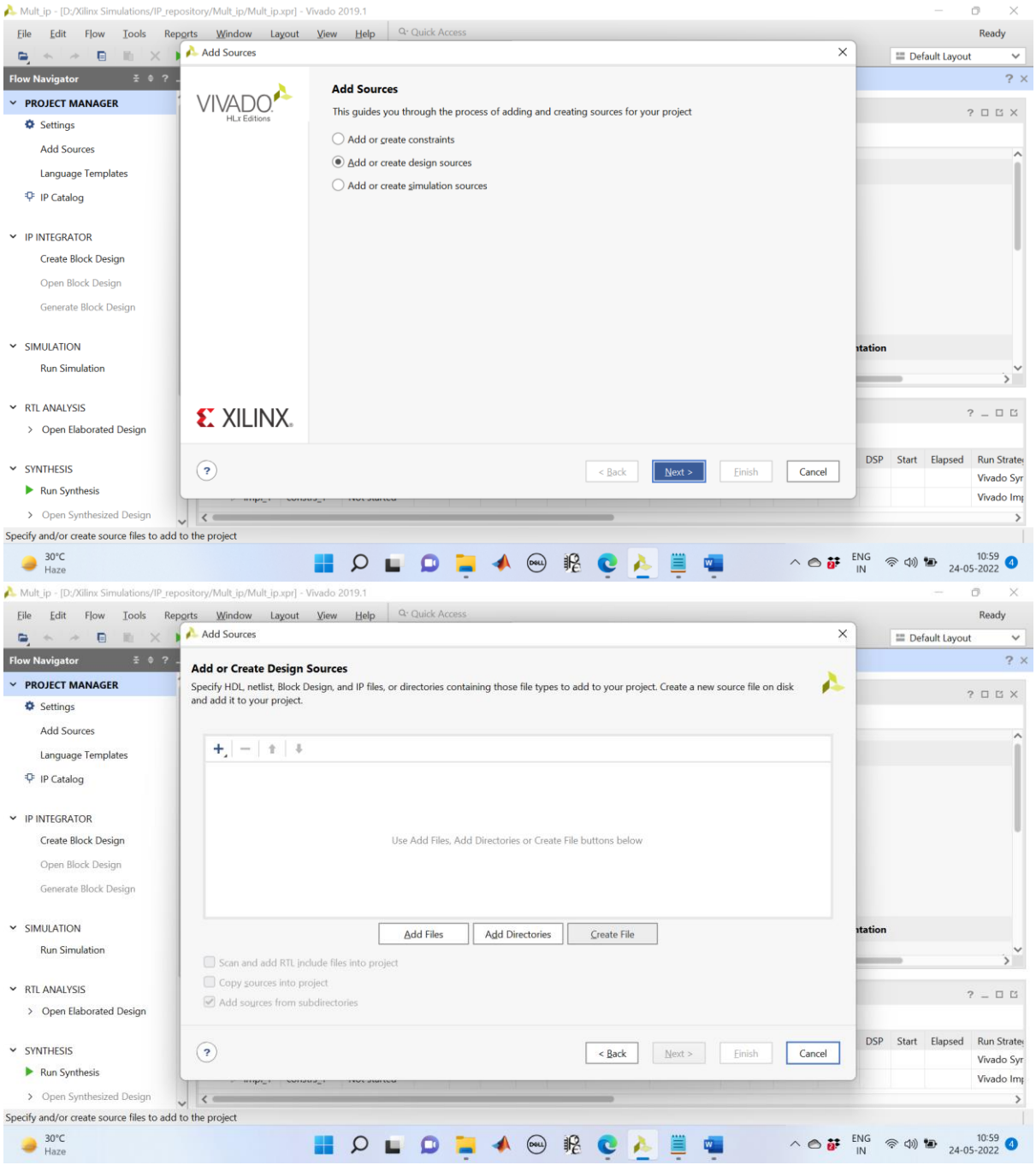
PROJECT MANAGER - Mult_ip
Sources
Design Sources
Properties... Ctrl+E
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Edit Constraints Sets...
Edit Simulation Sets...
Add Sources... Alt+A
Hierarchy
Properties
Select an object to see properties
Project Summary
Overview Dashboard
Settings Edit
Project name: Mult_ip
Project location: D:/Xilinx Simulations/IP_repository/Mult_ip
Product family: Artix-7
Project part: xc7a35tftg256-2
Top module name: Not defined
Target language: Verilog
Simulator language: Mixed
Synthesis
Implementation
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAMs URAM DSP Start Elapsed Run Strate
synth_1 constrs_1 Not started Vivado Syr
impl_1 constrs_1 Not started Vivado Imp
Specify and/or create source files to add to the project
30°C Haze
ENG IN
10:59 24-05-2022


Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
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Open Synthesized Design
Add Sources
VIVADO HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel
DSP
Start
Elapsed
Run Strate
Vivado Syr
Vivado Imp
Specify and/or create source files to add to the project
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Haze
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Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
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Open Synthesized Design
Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel
DSP
Start
Elapsed
Run Strate
Vivado Syr
Vivado Imp
Specify and/or create source files to add to the project
30°C
Haze
ENG
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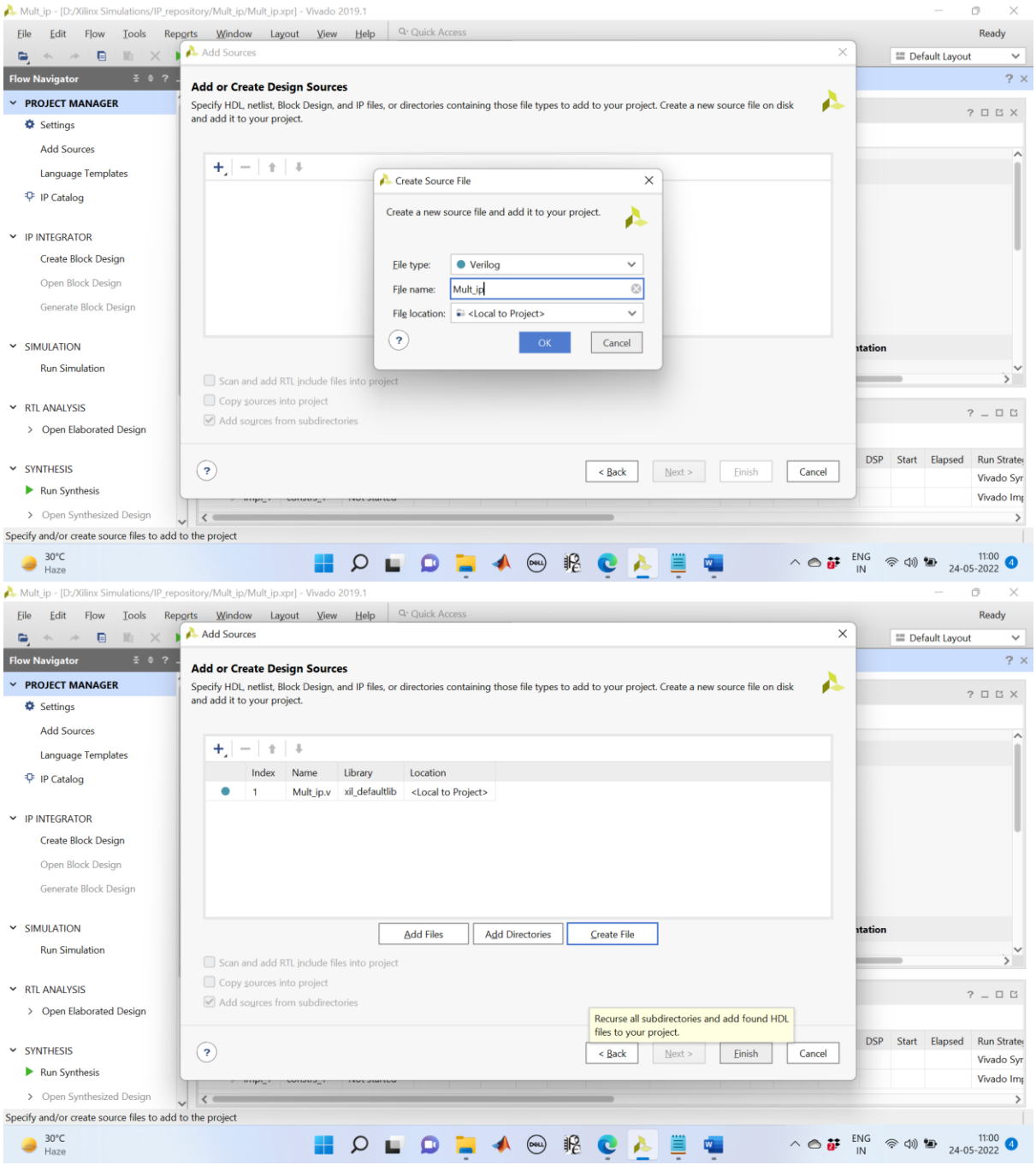
Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
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Open Synthesized Design
Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Create Source File
Create a new source file and add it to your project.
File type: Verilog
File name: Mult_ip
File location: <Local to Project>
OK
Cancel
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel
DSP
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Elapsed
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Vivado Syr
Vivado Imp
Specify and/or create source files to add to the project
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Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
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Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Index
Name
Library
Location
1
Mult_ip.v
xil_defaultlib
<Local to Project>
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Recurse all subdirectories and add found HDL files to your project.
< Back
Next >
Finish
Cancel
DSP
Start
Elapsed
Run Strate
Vivado Syr
Vivado Imp
Specify and/or create source files to add to the project
30°C
Haze
ENG
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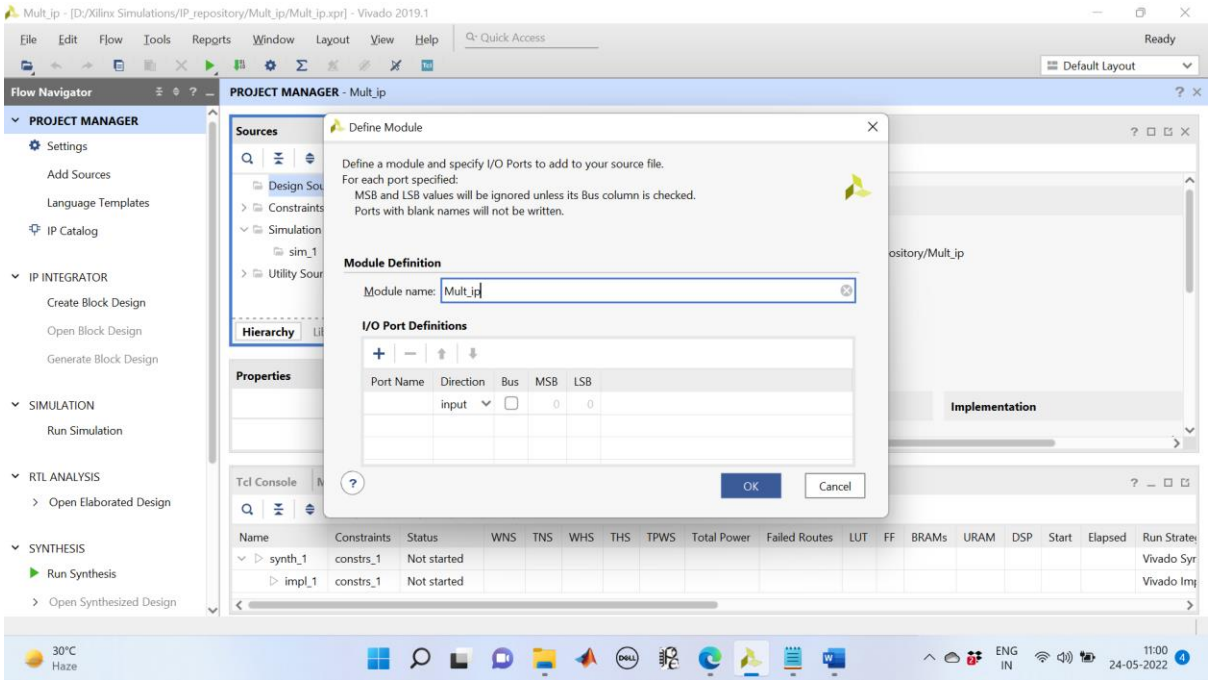
24-05-2022


Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
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PROJECT MANAGER - Mult_ip
Sources
Design Sources
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sim_1
Utility Sources
Hierarchy
Properties
Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name: Mult_ip
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
input
OK
Cancel
Implementation
Tcl Console
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAMs
URAM
DSP
Start
Elapsed
synth_1
constrs_1
Not started
impl_1
constrs_1
Not started
30°C
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ENG
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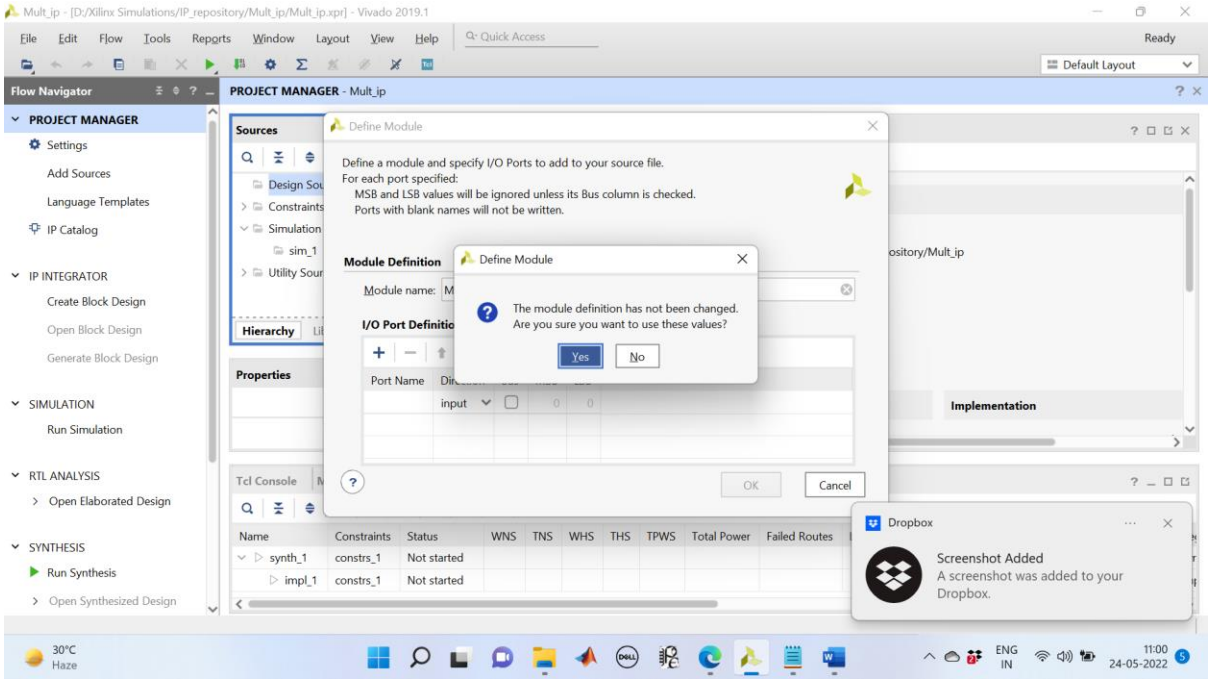
Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
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PROJECT MANAGER - Mult_ip
Sources
Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Define Module
The module definition has not been changed.
Are you sure you want to use these values?
Yes
No
Hierarchy
Properties
Port Name
input
OK
Cancel
Implementation
Tcl Console
Name
Constraints
Status
synth_1
constrs_1
Not started
impl_1
constrs_1
Not started
Dropbox
Screenshot Added
A screenshot was added to your Dropbox.
30°C
Haze
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IN
11:00
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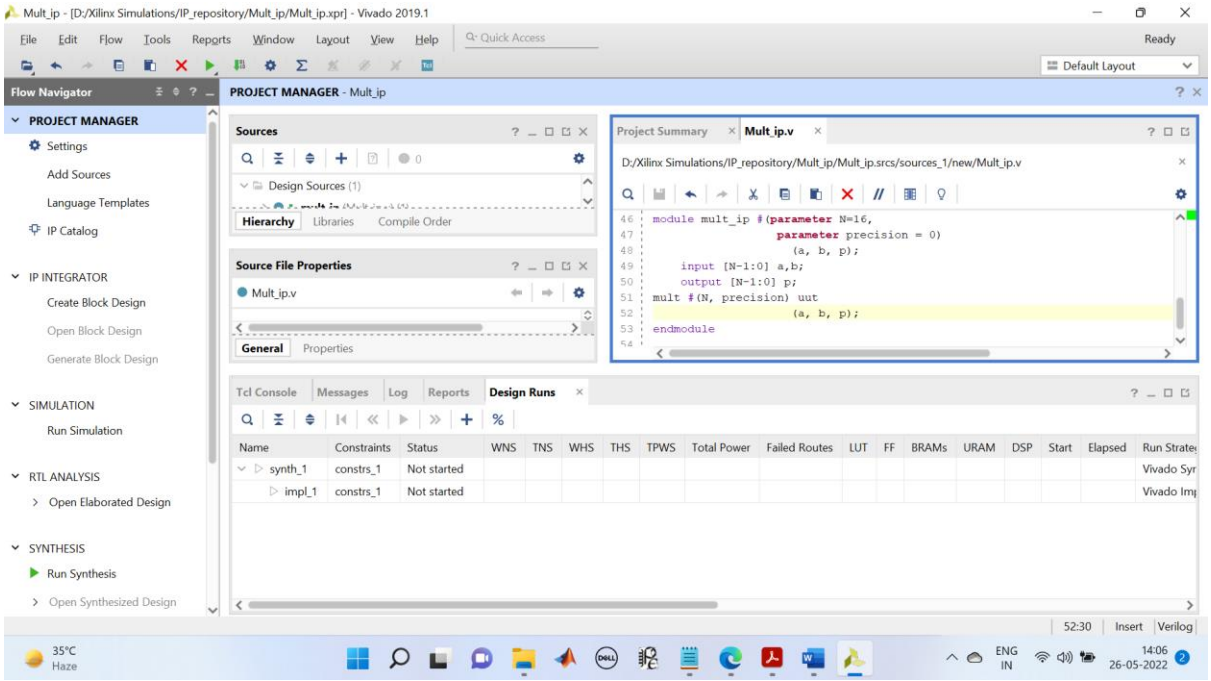
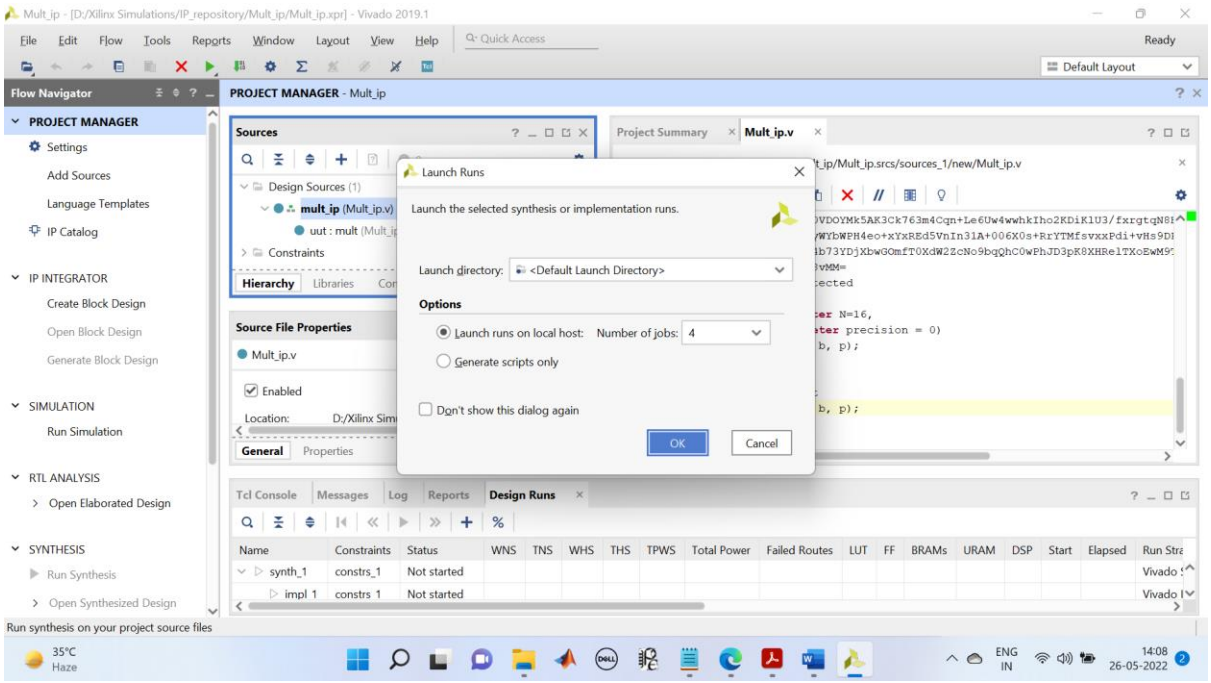
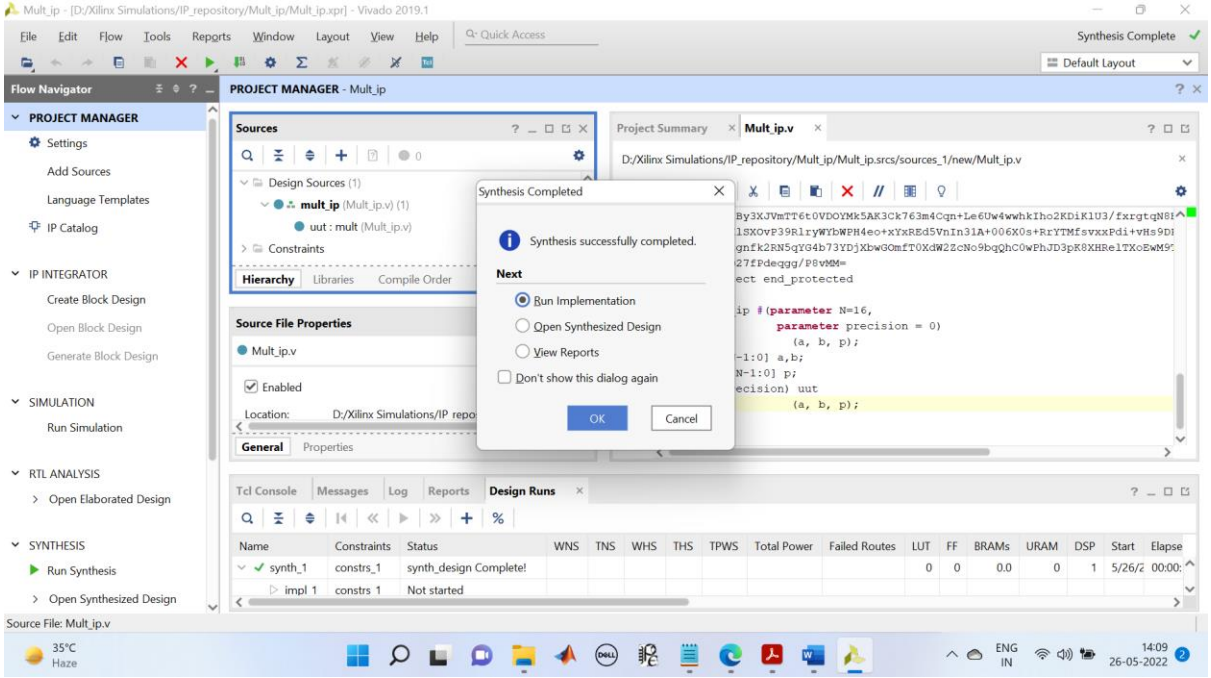
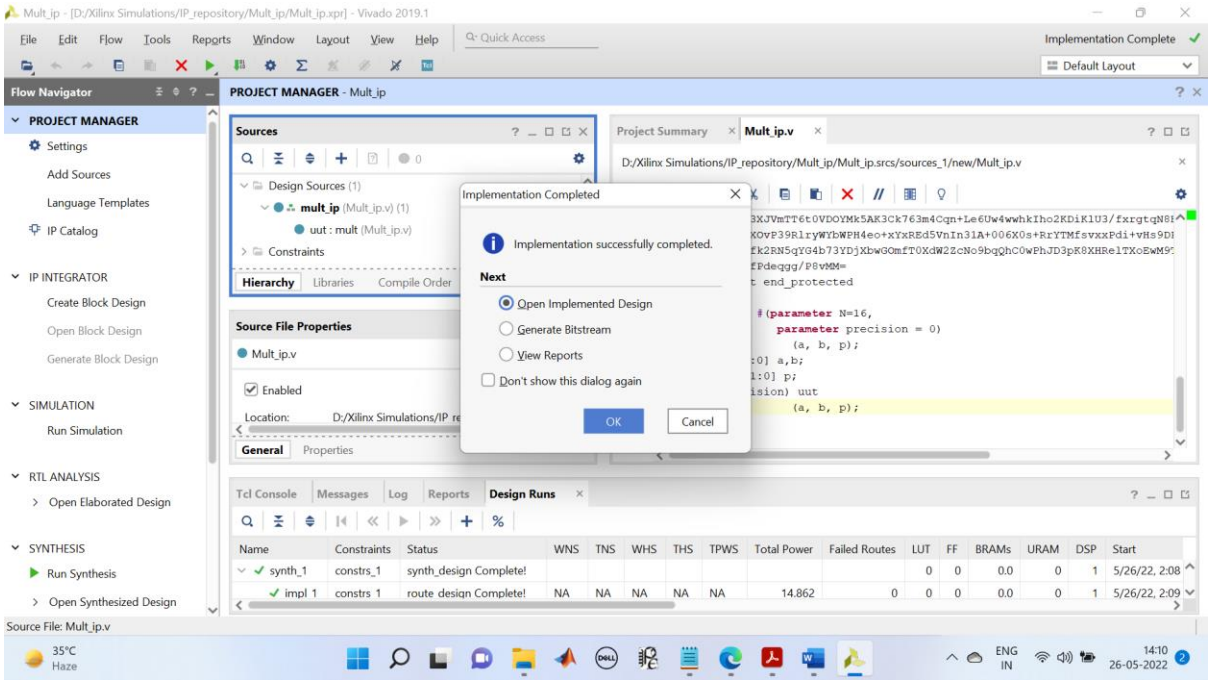


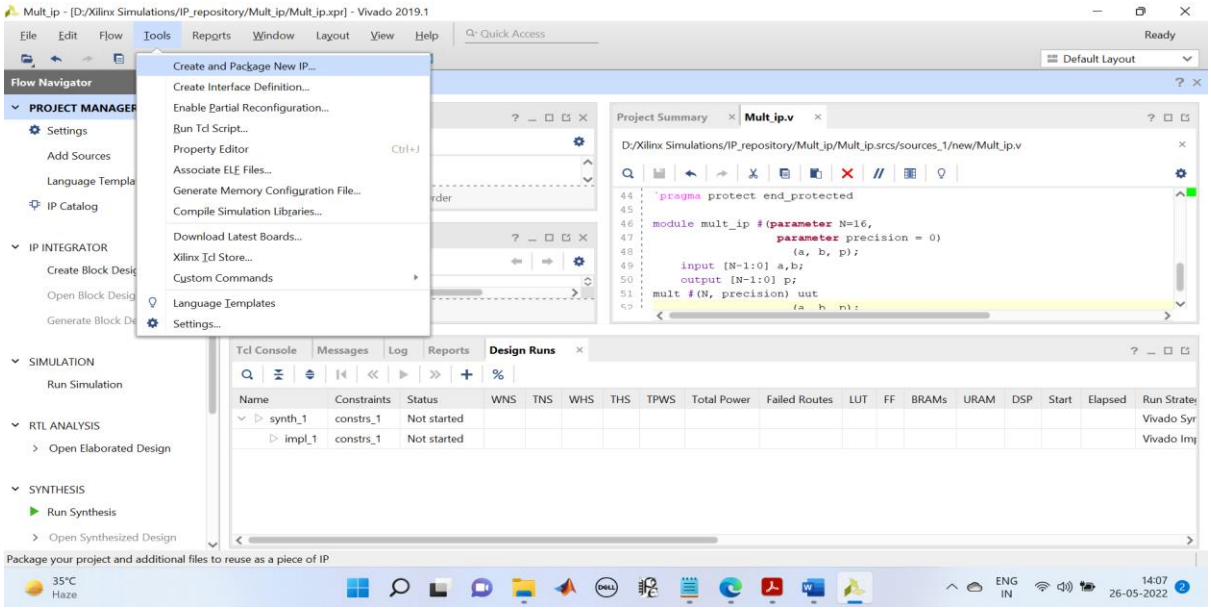
Do the functional simulation and Syhthesize the Verilog Module





Next do the implementation also. Bitstream generation also should be done. Once the Verilog code is fully verified then we can proceed to packaging.

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Create and Package New IP...
Create Interface Definition...
Enable Partial Reconfiguration...
Run Tcl Script...
Property Editor Ctrl+J
Associate ELF Files...
Generate Memory Configuration File...
Compile Simulation Libraries...
Download Latest Boards...
Xilinx Tcl Store...
Custom Commands
Language Templates
Settings...
Project Summary
Mult_ip.v
D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.srcs/sources_1/new/Mult_ip.v
`pragma protect end_protected
module mult_ip #(parameter N=16,
parameter precision = 0)
(a, b, p);
input [N-1:0] a,b;
output [N-1:0] p;
mult #(N, precision) uut
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAMs
URAM
DSP
Start
Elapsed
synth_1
constrs_1
Not started
impl_1
constrs_1
Not started
Package your project and additional files to reuse as a piece of IP
35°C
Haze
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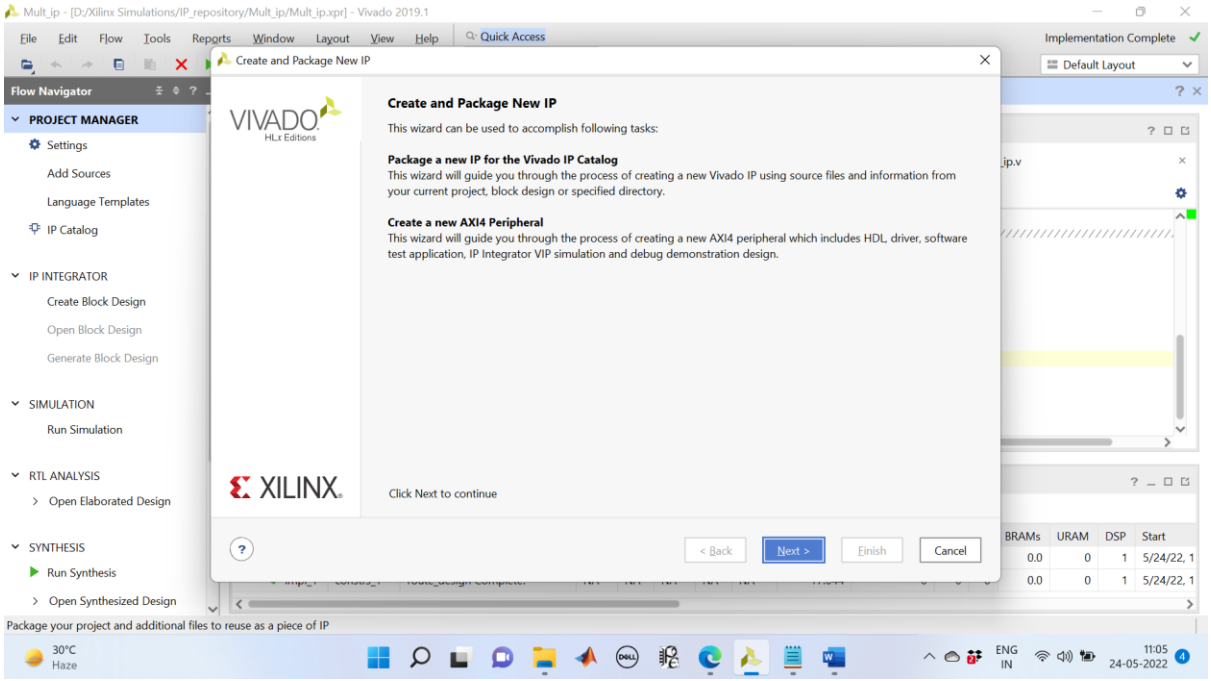
IN
14:07
26-05-2022


Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
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Create and Package New IP
VIVADO
HLx Editions
Create and Package New IP
This wizard can be used to accomplish following tasks:
Package a new IP for the Vivado IP Catalog
This wizard will guide you through the process of creating a new Vivado IP using source files and information from your current project, block design or specified directory.
Create a new AXI4 Peripheral
This wizard will guide you through the process of creating a new AXI4 peripheral which includes HDL, driver, software test application, IP Integrator VIP simulation and debug demonstration design.
XILINX
Click Next to continue
< Back
Next >
Finish
Cancel
BRAMs
URAM
DSP
Start
0.0
0
1
5/24/22, 1
Package your project and additional files to reuse as a piece of IP
30°C
Haze
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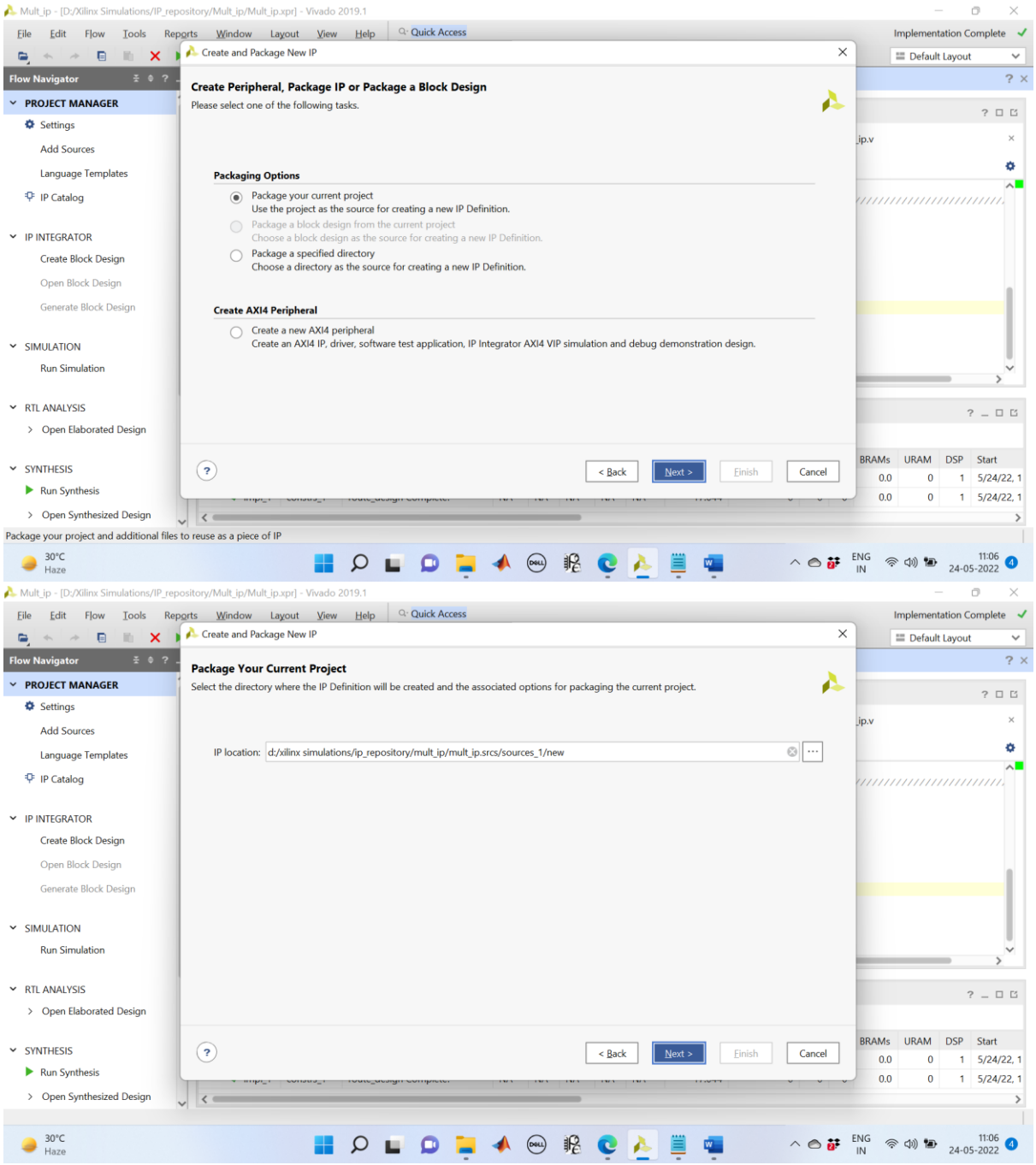
Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
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RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Create and Package New IP
Create Peripheral, Package IP or Package a Block Design
Please select one of the following tasks.
Packaging Options
Package your current project
Use the project as the source for creating a new IP Definition.
Package a block design from the current project
Choose a block design as the source for creating a new IP Definition.
Package a specified directory
Choose a directory as the source for creating a new IP Definition.
Create AXI4 Peripheral
Create a new AXI4 peripheral
Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design.
< Back
Next >
Finish
Cancel
BRAMs URAM DSP Start
0.0 0 1 5/24/22, 1
0.0 0 1 5/24/22, 1
Package your project and additional files to reuse as a piece of IP
30°C Haze
ENG IN
11:06 24-05-2022

Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
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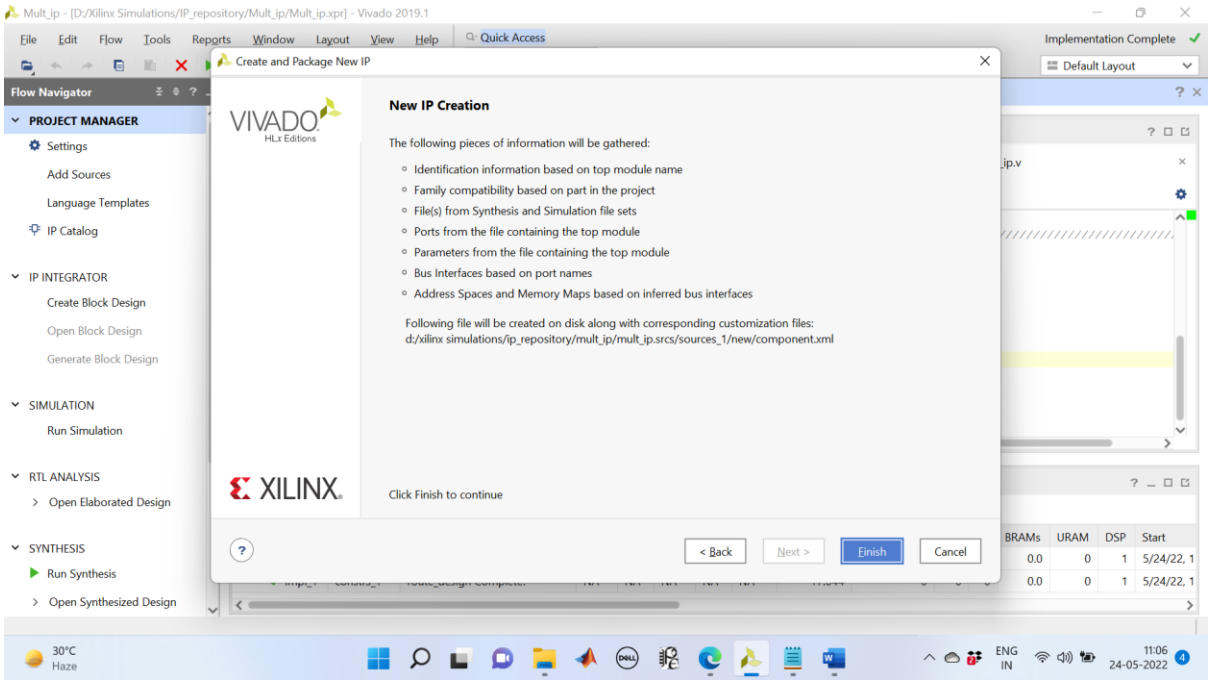
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Create and Package New IP
Package Your Current Project
Select the directory where the IP Definition will be created and the associated options for packaging the current project.
IP location: d:/xilinx simulations/ip_repository/mult_ip/mult_ip.srcs/sources_1/new
< Back
Next >
Finish
Cancel
BRAMs URAM DSP Start
0.0 0 1 5/24/22, 1
0.0 0 1 5/24/22, 1
30°C Haze
ENG IN
11:06 24-05-2022


Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
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Default Layout
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SYNTHESIS
Run Synthesis
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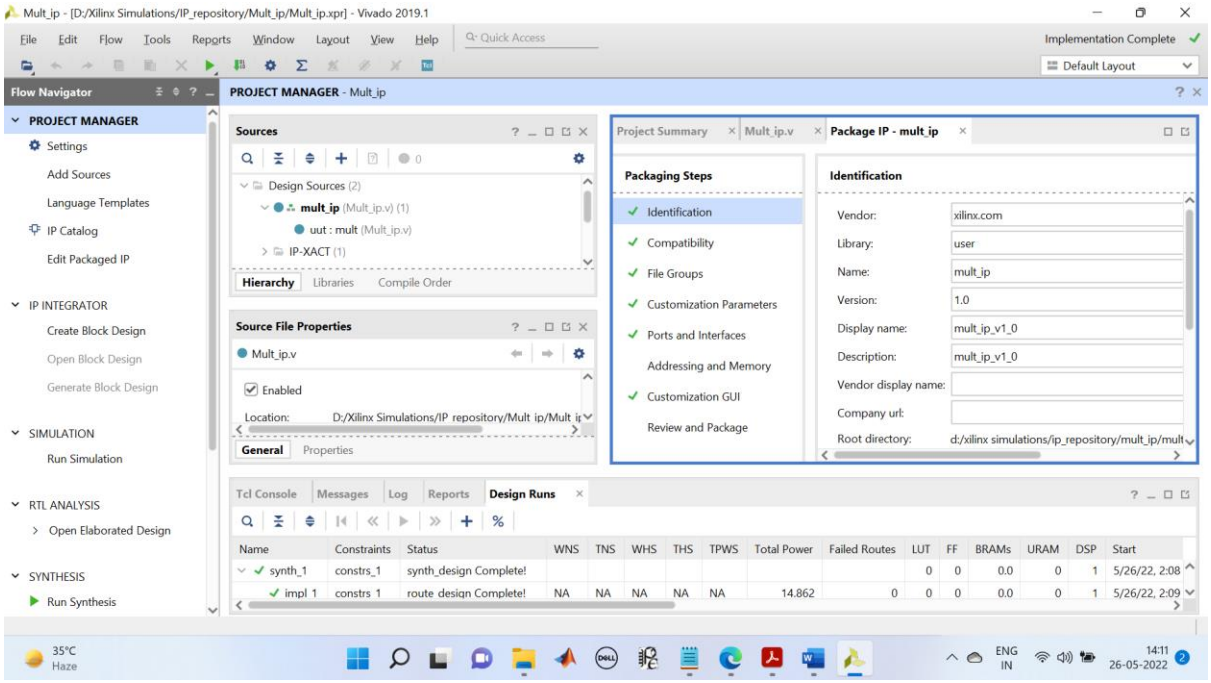
Create and Package New IP
VIVADO HLx Editions
New IP Creation
The following pieces of information will be gathered:
Identification information based on top module name
Family compatibility based on part in the project
File(s) from Synthesis and Simulation file sets
Ports from the file containing the top module
Parameters from the file containing the top module
Bus Interfaces based on port names
Address Spaces and Memory Maps based on inferred bus interfaces
Following file will be created on disk along with corresponding customization files:
d:/xilinx simulations/ip_repository/mult_ip/mult_ip.srcs/sources_1/new/component.xml
XILINX
Click Finish to continue
< Back
Next >
Finish
Cancel
BRAMs URAM DSP Start
0.0 0 1 5/24/22, 1
0.0 0 1 5/24/22, 1
30°C Haze
ENG IN
11:06 24-05-2022


Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
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Default Layout
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SIMULATION
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RTL ANALYSIS
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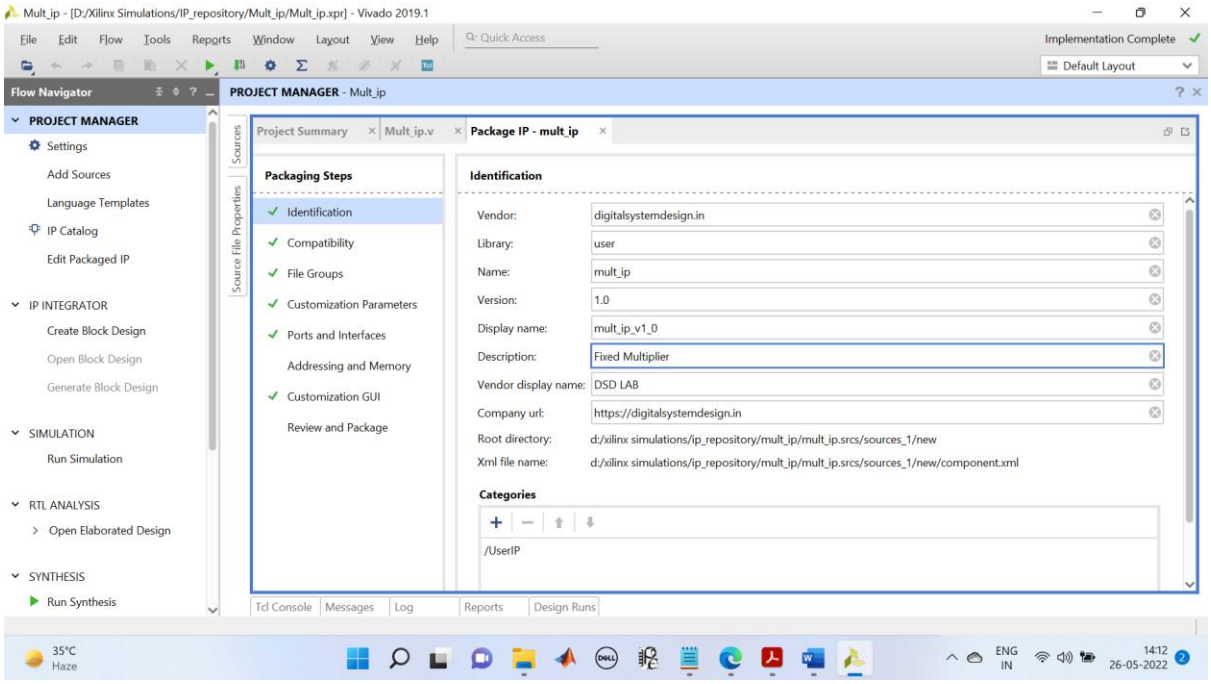
SYNTHESIS
Run Synthesis
Sources
Design Sources (2)
mult_ip (Mult_ip.v) (1)
uut : mult (Mult_ip.v)
IP-XACT (1)
Hierarchy Libraries Compile Order
Source File Properties
Mult_ip.v
Enabled
Location: D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip
General Properties
Project Summary
Mult_ip.v
Package IP - mult_ip
Packaging Steps
Identification
Compatibility
File Groups
Customization Parameters
Ports and Interfaces
Addressing and Memory
Customization GUI
Review and Package
Identification
Vendor: xilinx.com
Library: user
Name: mult_ip
Version: 1.0
Display name: mult_ip_v1_0
Description: mult_ip_v1_0
Vendor display name:
Company url:
Root directory: d:/xilinx simulations/ip_repository/mult_ip/mult
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAMs URAM DSP Start
synth_1 constrs_1 synth_design Complete! 0 0 0.0 0 1 5/26/22, 2:08
impl 1 constrs 1 route design Complete! NA NA NA NA NA 14.862 0 0 0 0.0 0 1 5/26/22, 2:09
35°C Haze
ENG IN
14:11 26-05-2022


Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
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Mult_ip.v
Package IP - mult_ip
Packaging Steps
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Compatibility
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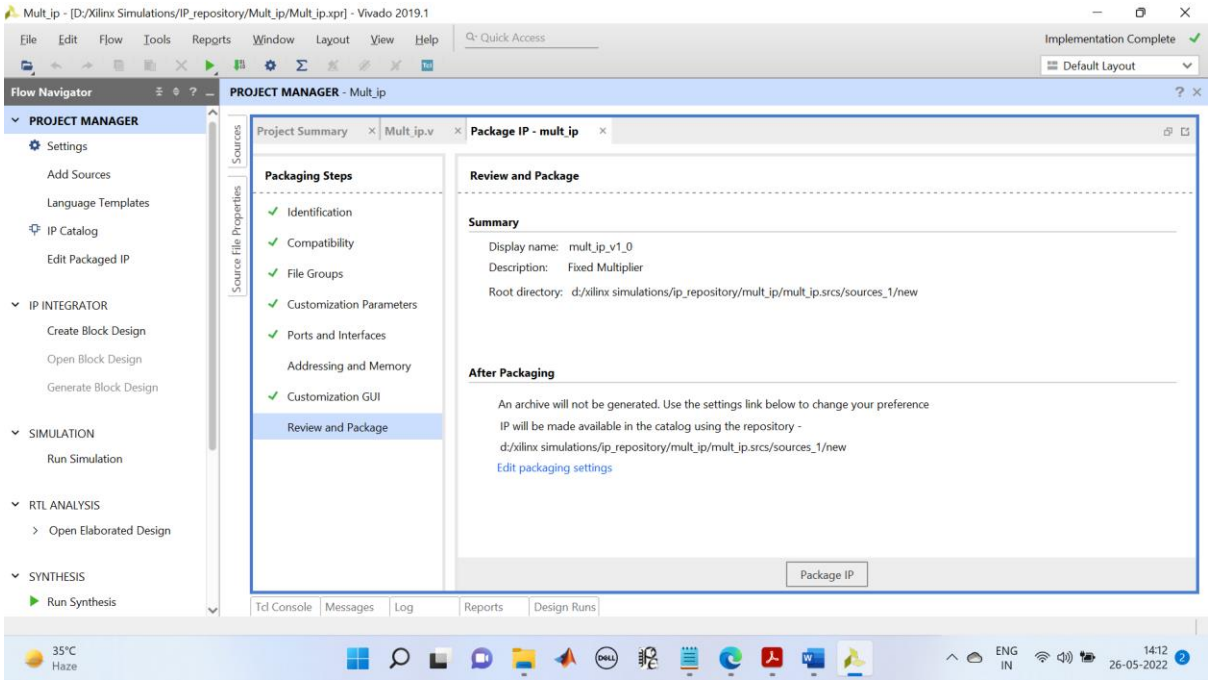
Customization Parameters
Ports and Interfaces
Addressing and Memory
Customization GUI
Review and Package
Identification
Vendor: digitalsystemdesign.in
Library: user
Name: mult_ip
Version: 1.0
Display name: mult_ip_v1_0
Description: Fixed Multiplier
Vendor display name: DSD LAB
Company url: https://digitalsystemdesign.in
Root directory: d:/xilinx simulations/ip_repository/mult_ip/mult_ip.srcs/sources_1/new
Xml file name: d:/xilinx simulations/ip_repository/mult_ip/mult_ip.srcs/sources_1/new/component.xml
Categories
/UserIP
Tcl Console Messages Log Reports Design Runs
35°C Haze
ENG IN
14:12 26-05-2022


Mult_ip - [D:/Xilinx Simulations/IP_repository/Mult_ip/Mult_ip.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
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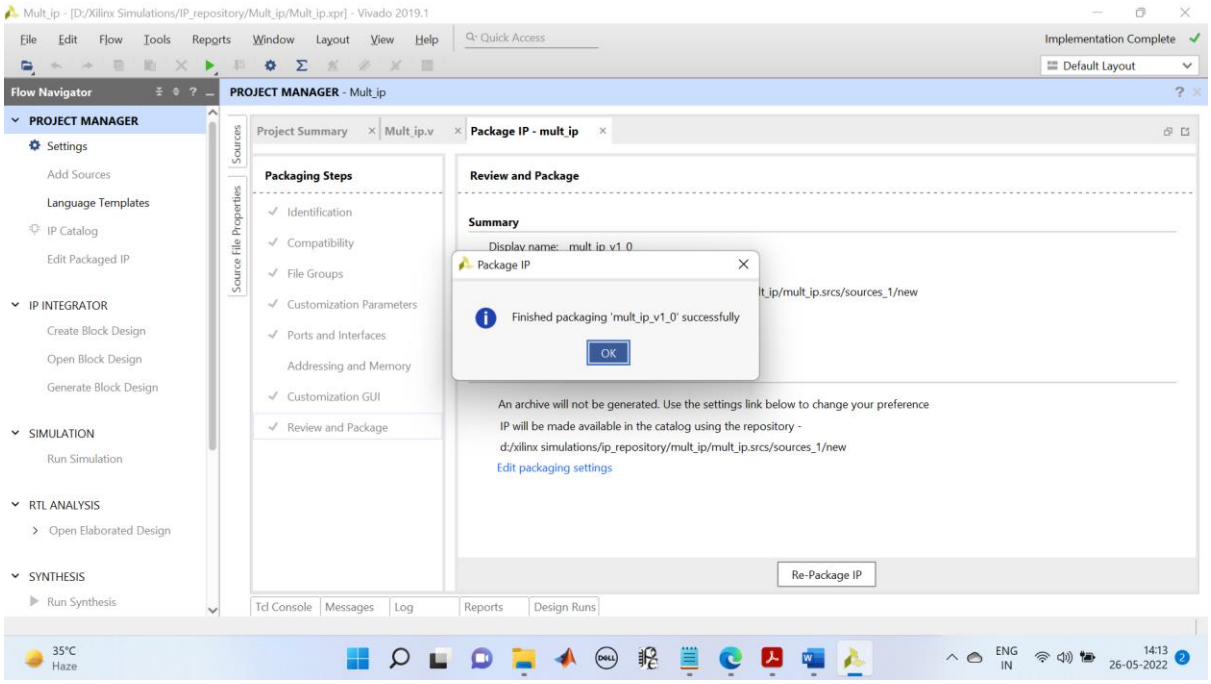
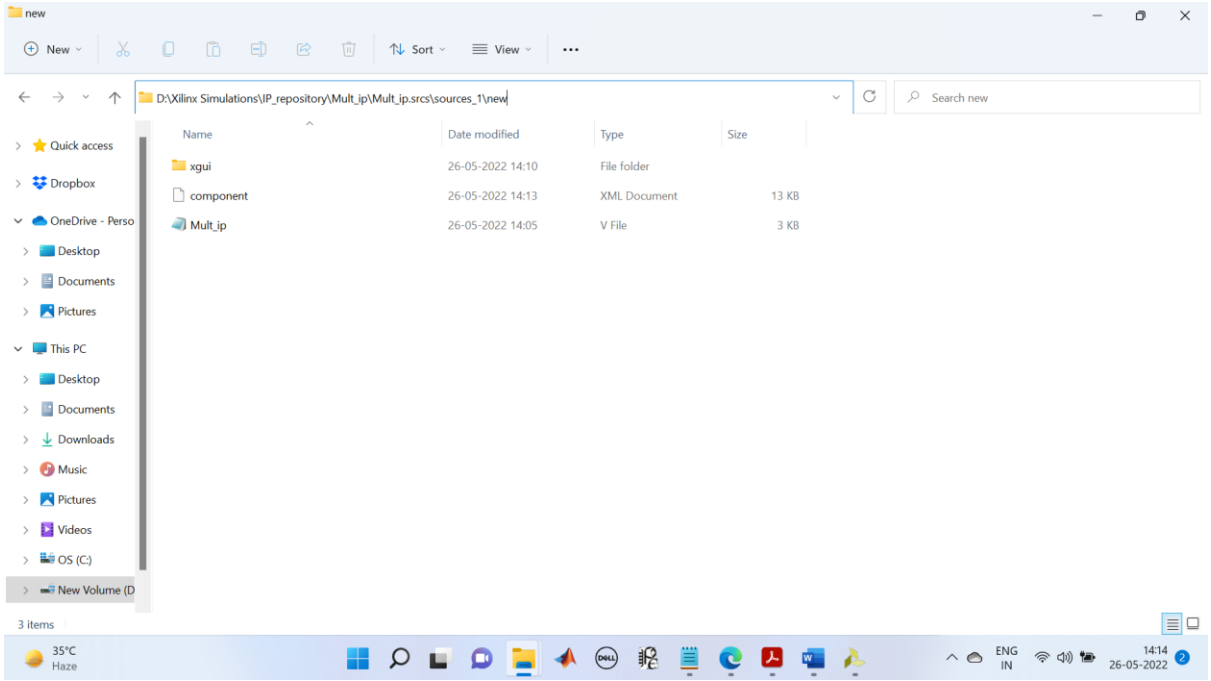
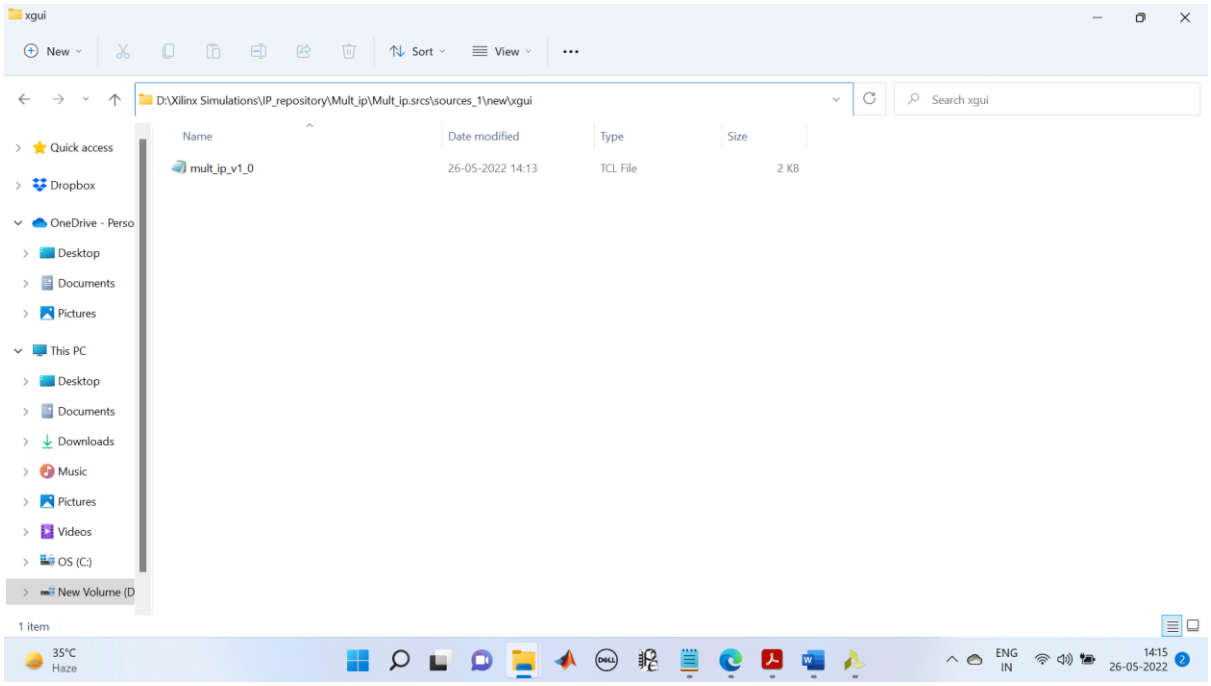
SYNTHESIS
Run Synthesis
PROJECT MANAGER - Mult_ip
Project Summary
Mult_ip.v
Package IP - mult_ip
Packaging Steps
Identification
Compatibility
File Groups
Customization Parameters
Ports and Interfaces
Addressing and Memory
Customization GUI
Review and Package
Review and Package
Summary
Display name: mult_ip_v1_0
Description: Fixed Multiplier
Root directory: d:/xilinx simulations/ip_repository/mult_ip/mult_ip.srcs/sources_1/new
After Packaging
An archive will not be generated. Use the settings link below to change your preference
IP will be made available in the catalog using the repository -
d:/xilinx simulations/ip_repository/mult_ip/mult_ip.srcs/sources_1/new
Edit packaging settings
Package IP
Tcl Console Messages Log Reports Design Runs
35°C Haze
ENG IN
14:12 26-05-2022

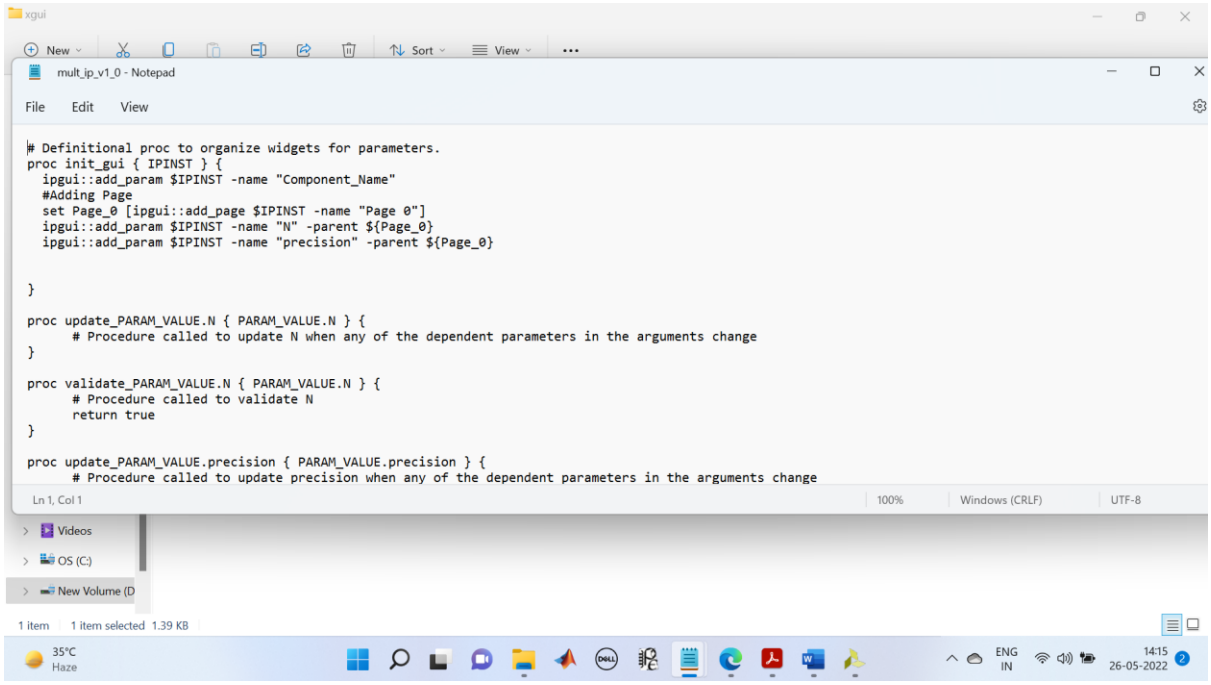


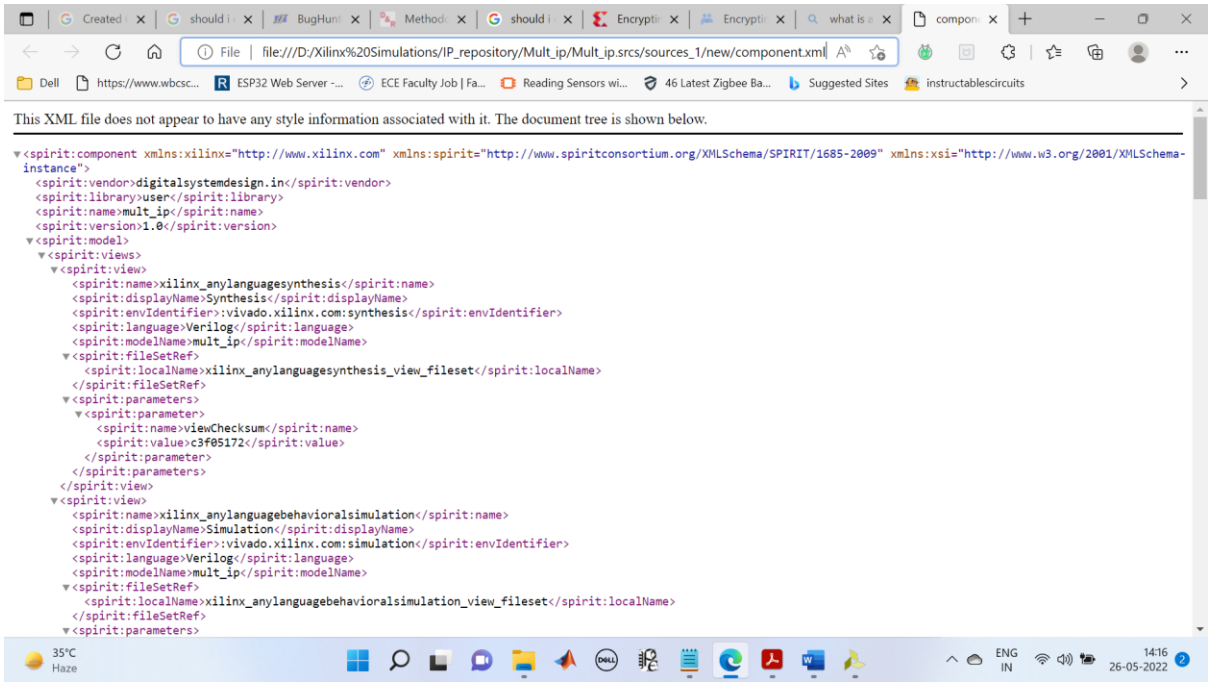
Two another important files are created. One XML file which is responsible for GUI and another is tcl file which is responsible for interface between the Verilog file and the GUI.





This is the .tcl file which was generated.





This is the XML file of the IP.