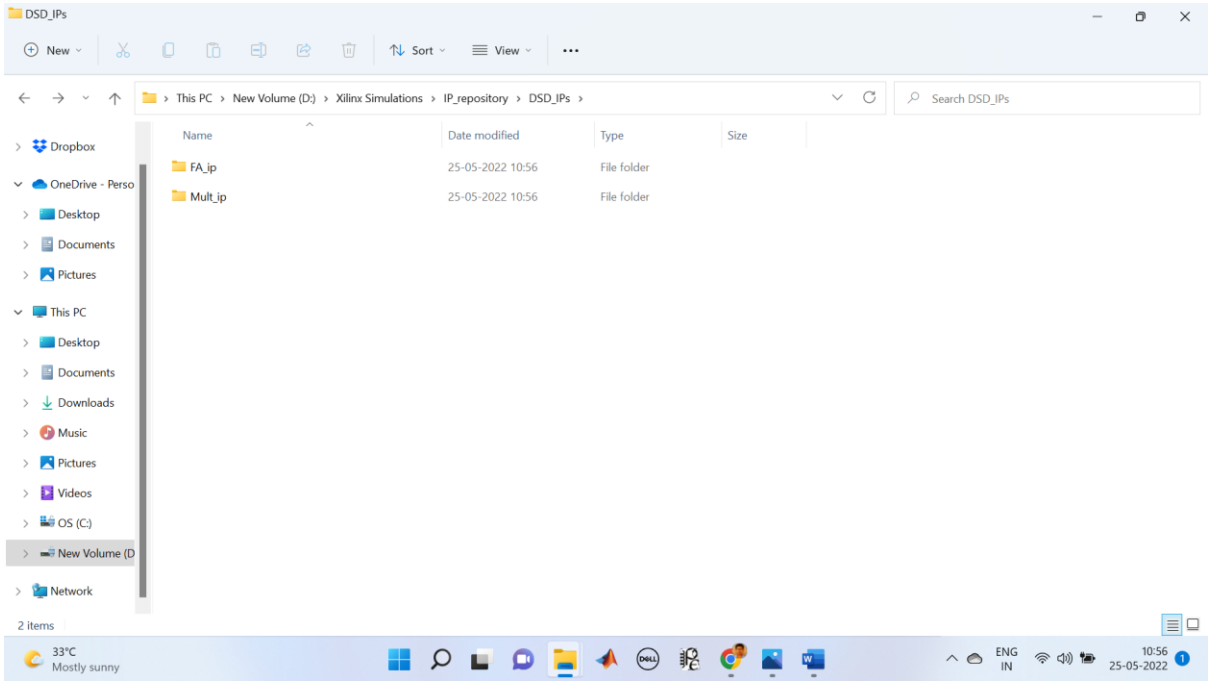
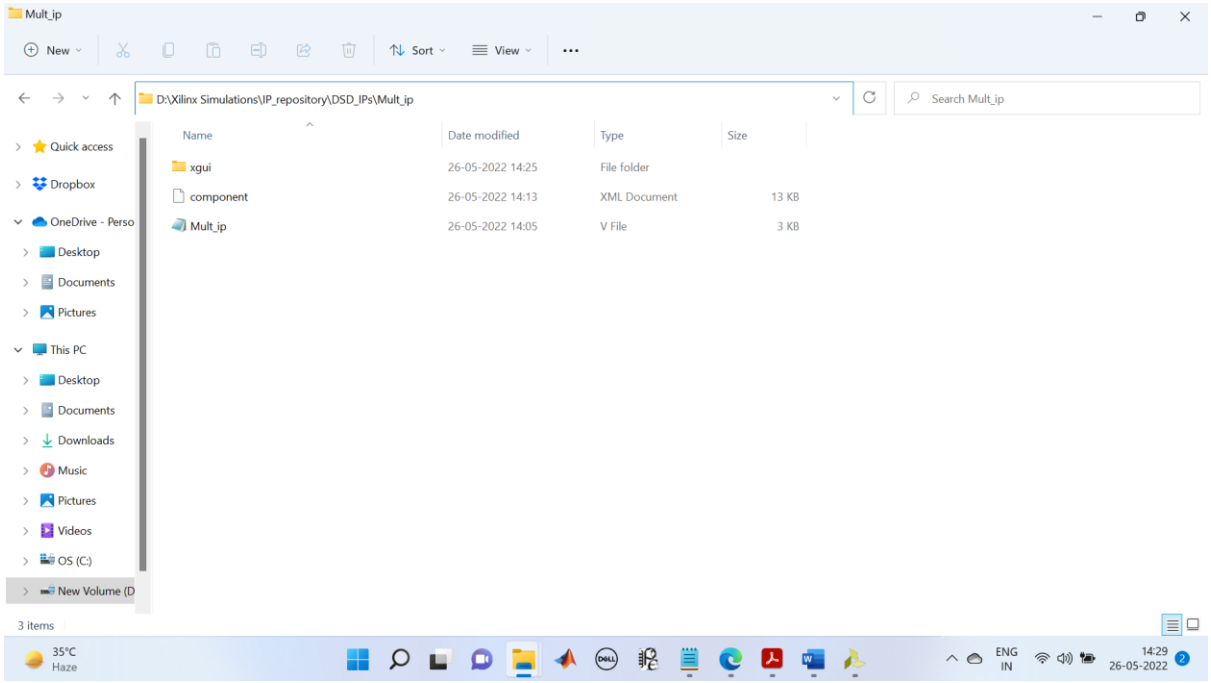
How to use DSD LAB IPs in a Block Design

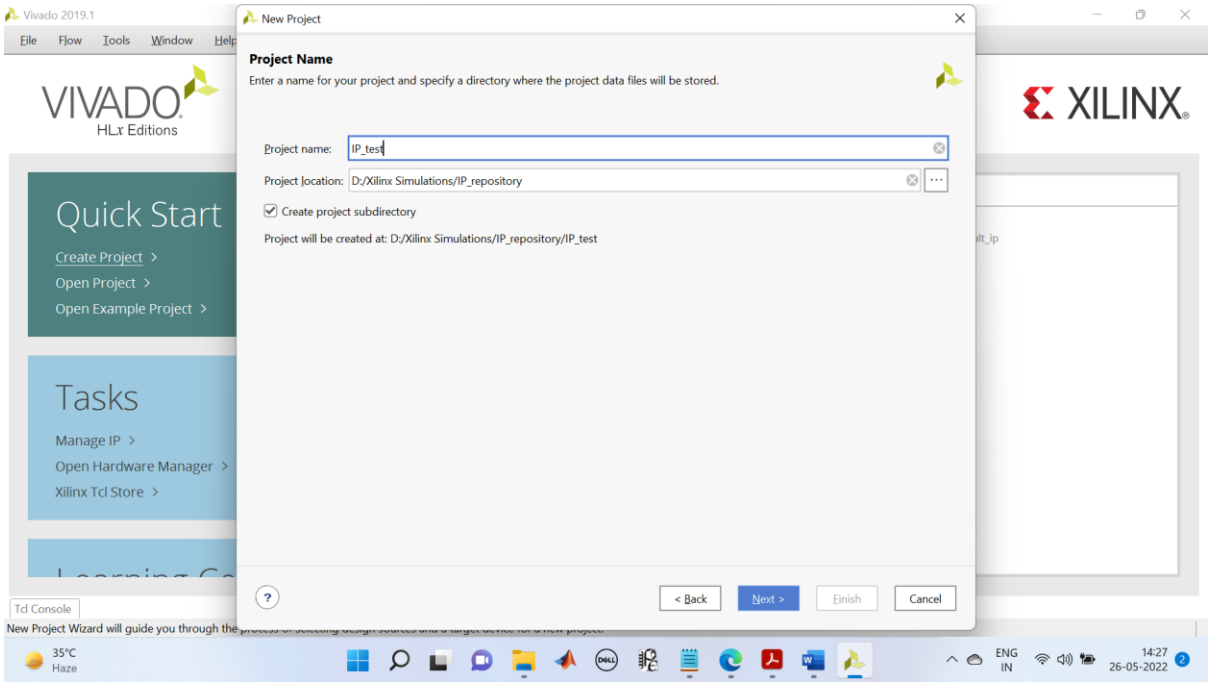
1. All the IPs from the digitalsystemdesign.in can be stored in a folder as shown below.

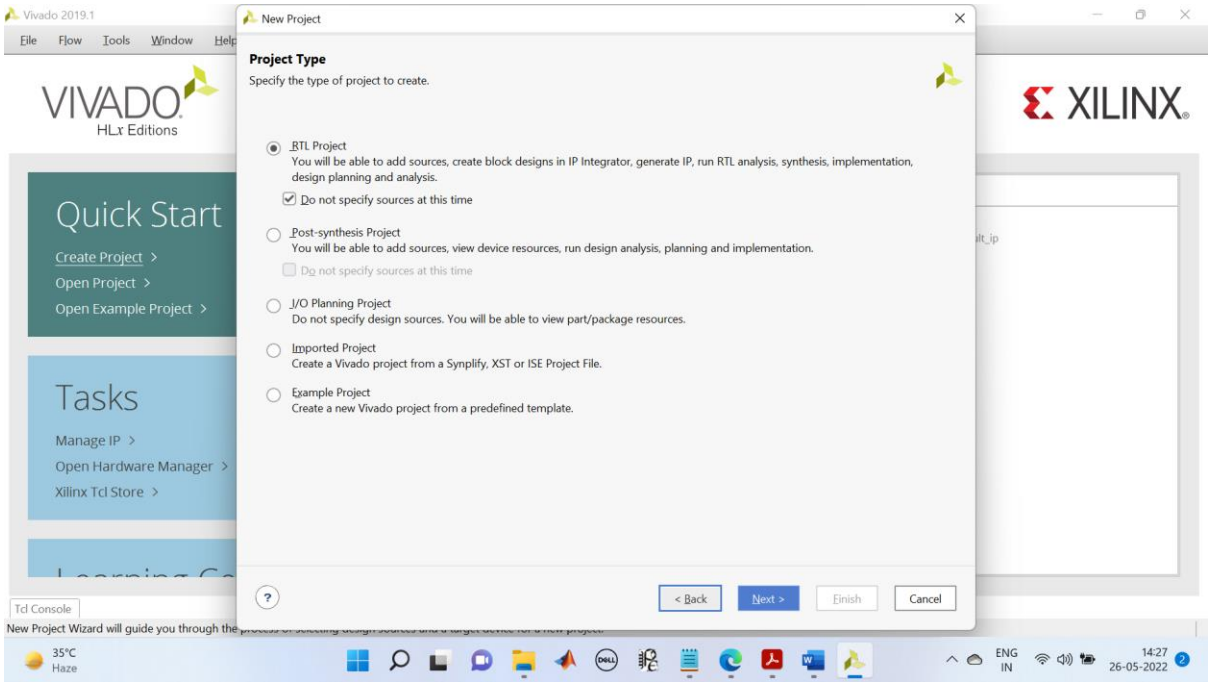


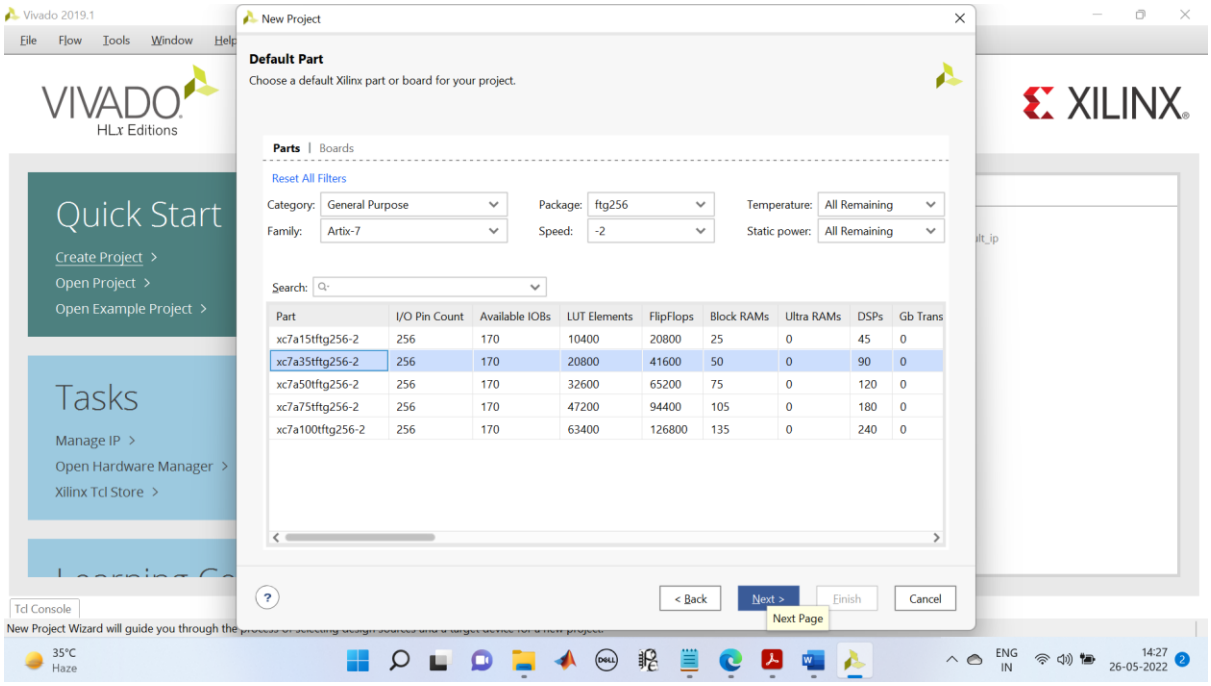
2. Here in this tutorial, the multiplier IP will be tested. This is a fixed-point rectangular multiplier whose precision and data-width can be varied. The folder contains two files, one is component files which is an .xml file responsible for the IP GUI. It also contains the encrypted Verilog source file. The xgui file contains the .tcl file of the IP.

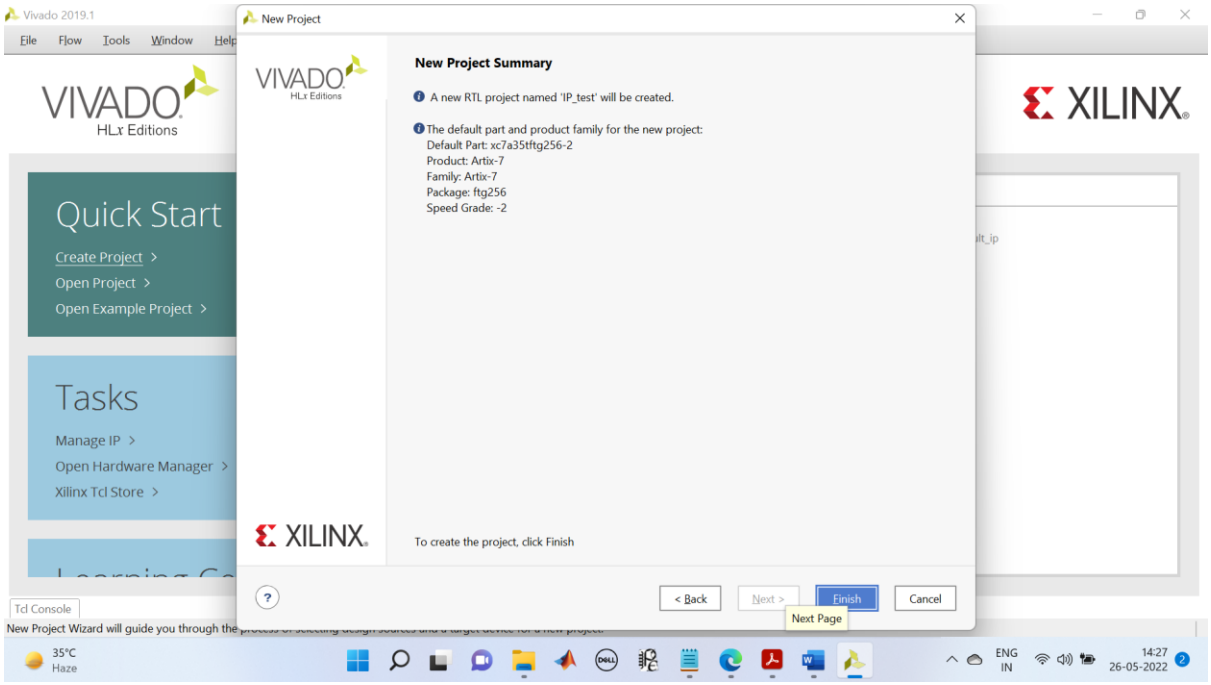


3. Open a new project where we are going to use the IP.

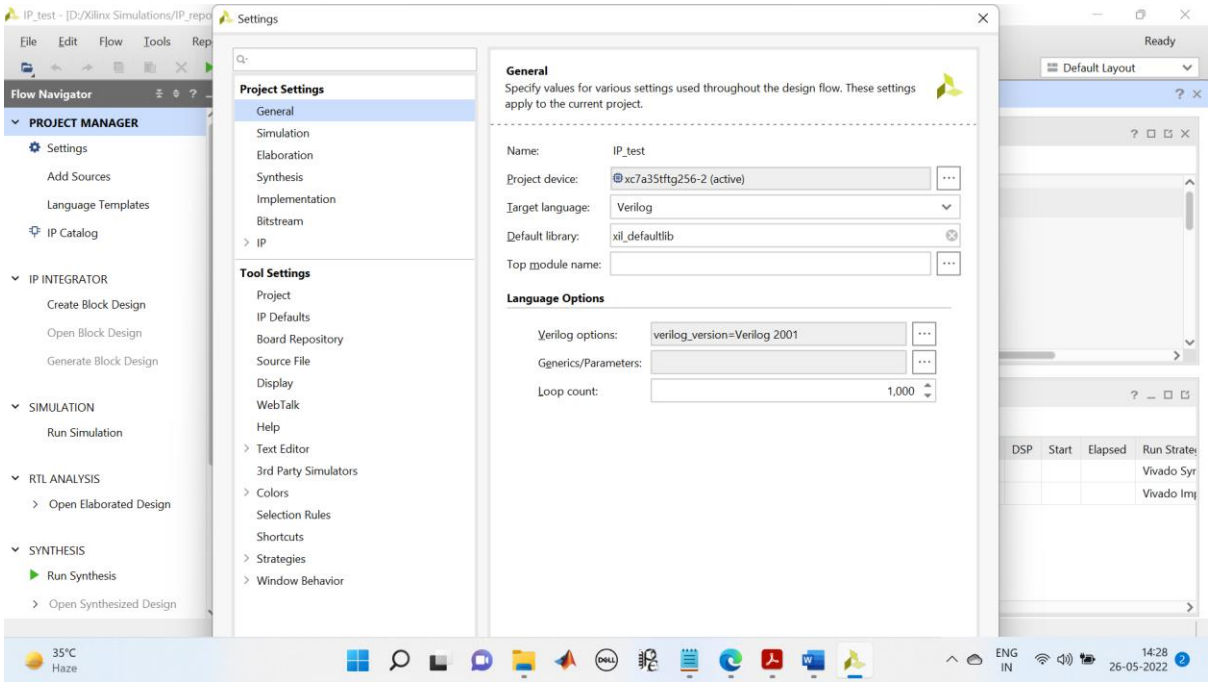

Vivado 2019.1
File Flow Tools Window Help
VIVADO
HLx Editions
XILINX
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name: IP_test
Project location: D:/Xilinx Simulations/IP_repository
Create project subdirectory
Project will be created at: D:/Xilinx Simulations/IP_repository/IP_test
< Back
Next >
Finish
Cancel
Tcl Console
New Project Wizard will guide you through the
35°C
Haze
ENG
IN
14:27
26-05-2022

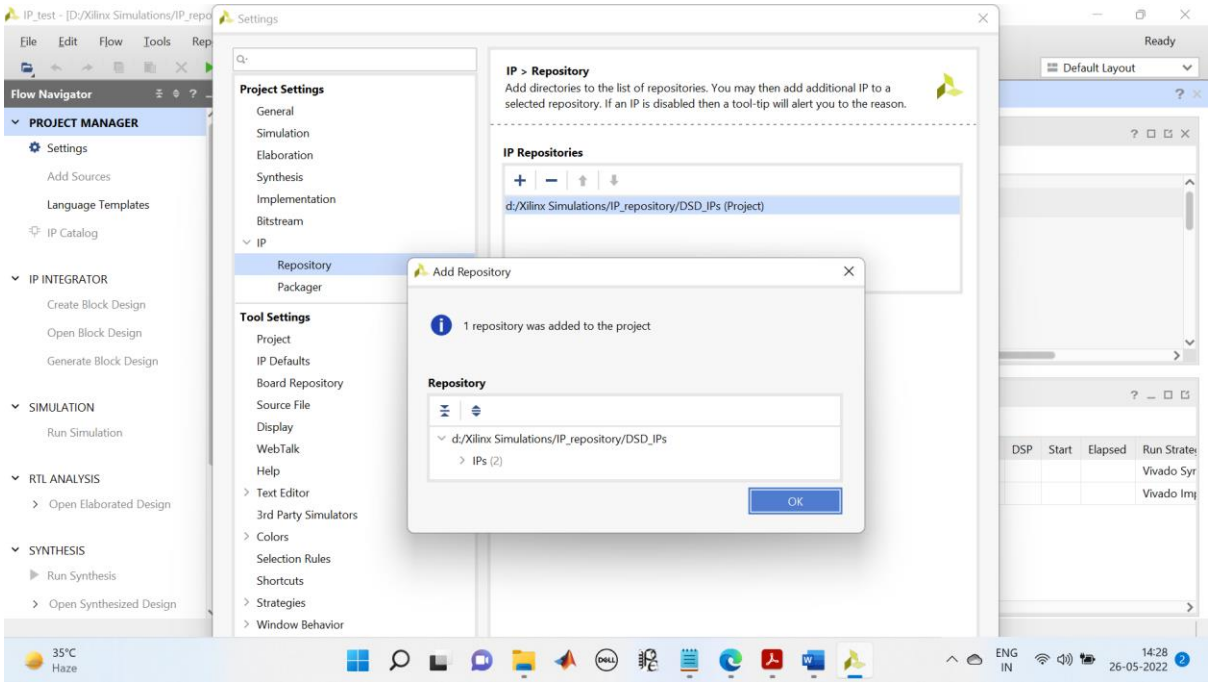

Vivado 2019.1
File Flow Tools Window Help
VIVADO
HLx Editions
XILINX
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel
Tcl Console
New Project Wizard will guide you through the
35°C
Haze
ENG
IN
14:27
26-05-2022





4. Go to settings and give the path of the folder where all the IPs are stored.


Settings
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
Tool Settings
Project
IP Defaults
Board Repository
Source File
Display
WebTalk
Help
Text Editor
3rd Party Simulators
Colors
Selection Rules
Shortcuts
Strategies
Window Behavior
General
Specify values for various settings used throughout the design flow. These settings apply to the current project.
Name: IP_test
Project device: xc7a35tftg256-2 (active)
Target language: Verilog
Default library: xil_defaultlib
Top module name:
Language Options
Verilog options: verilog_version=Verilog 2001
Generics/Parameters:
Loop count: 1,000
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Ready
Default Layout
DSP
Start
Elapsed
Run Strate
Vivado Syr
Vivado Imp
35°C
Haze
ENG
IN
14:28
26-05-2022


Settings
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
Repository
Packager
Tool Settings
Project
IP Defaults
Board Repository
Source File
Display
WebTalk
Help
Text Editor
3rd Party Simulators
Colors
Selection Rules
Shortcuts
Strategies
Window Behavior
IP > Repository
Add directories to the list of repositories. You may then add additional IP to a selected repository. If an IP is disabled then a tool-tip will alert you to the reason.
IP Repositories
d:/Xilinx Simulations/IP_repository/DSD_IPs (Project)
Add Repository
1 repository was added to the project
Repository
d:/Xilinx Simulations/IP_repository/DSD_IPs
IPs (2)
OK
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Ready
Default Layout
DSP
Start
Elapsed
Run Strate
Vivado Syr
Vivado Imp
35°C
Haze
ENG
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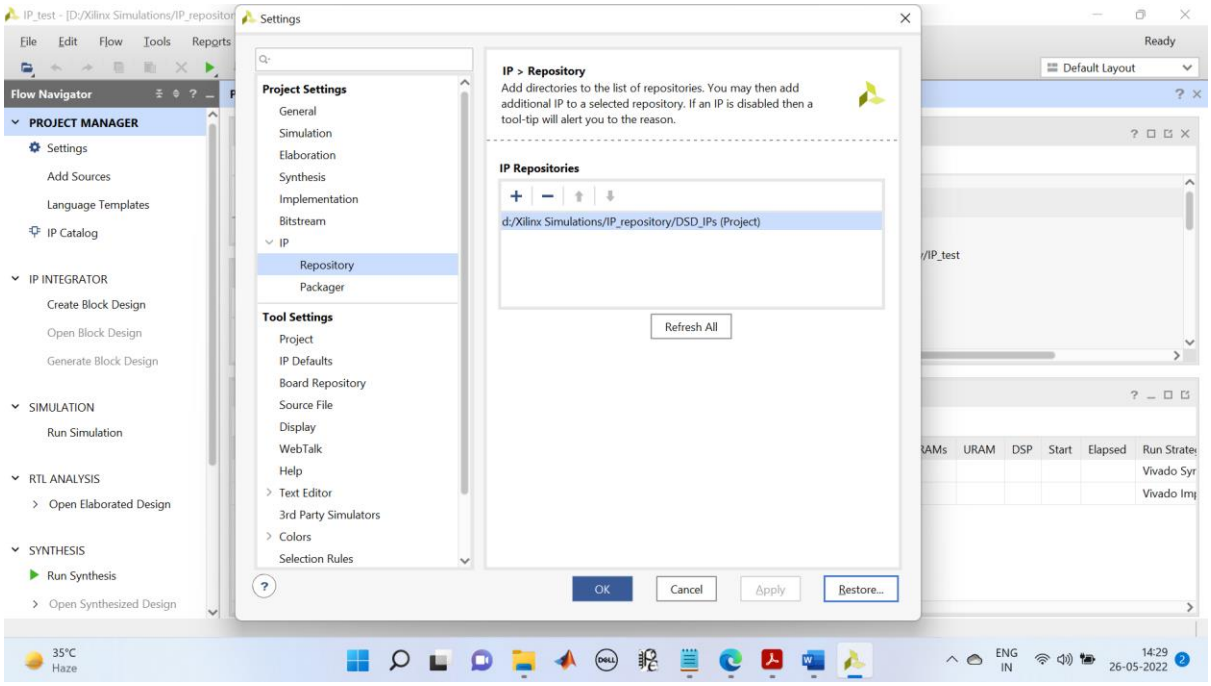
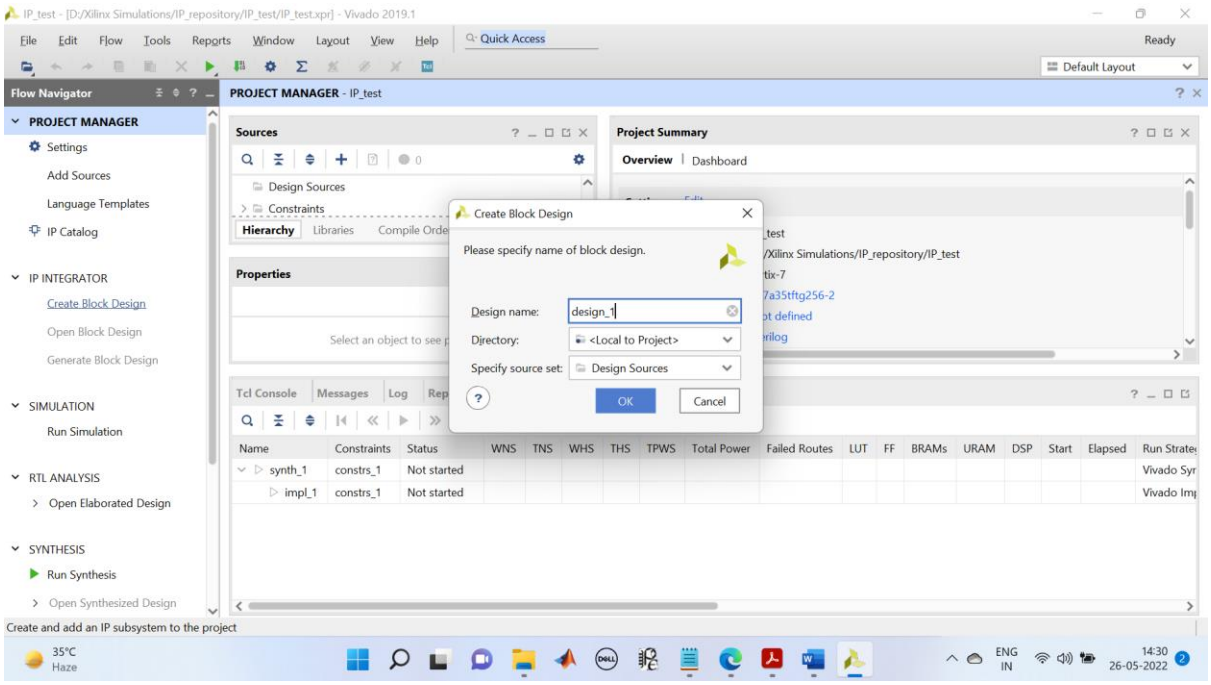
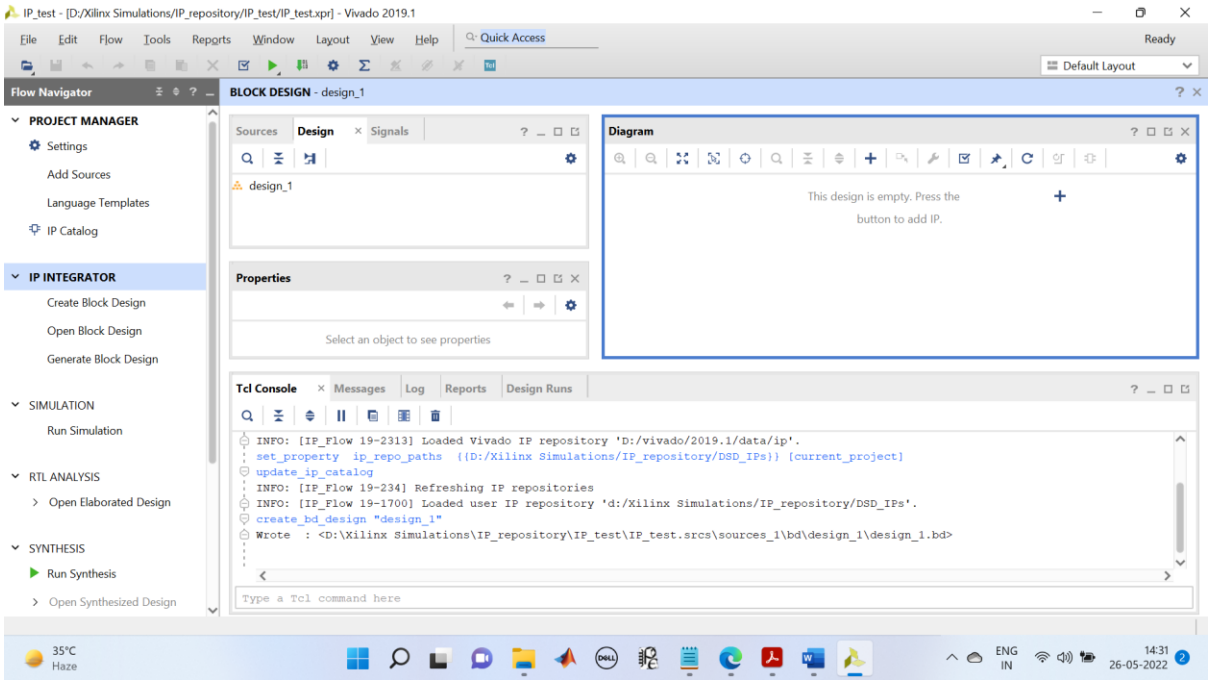
14:28
26-05-2022

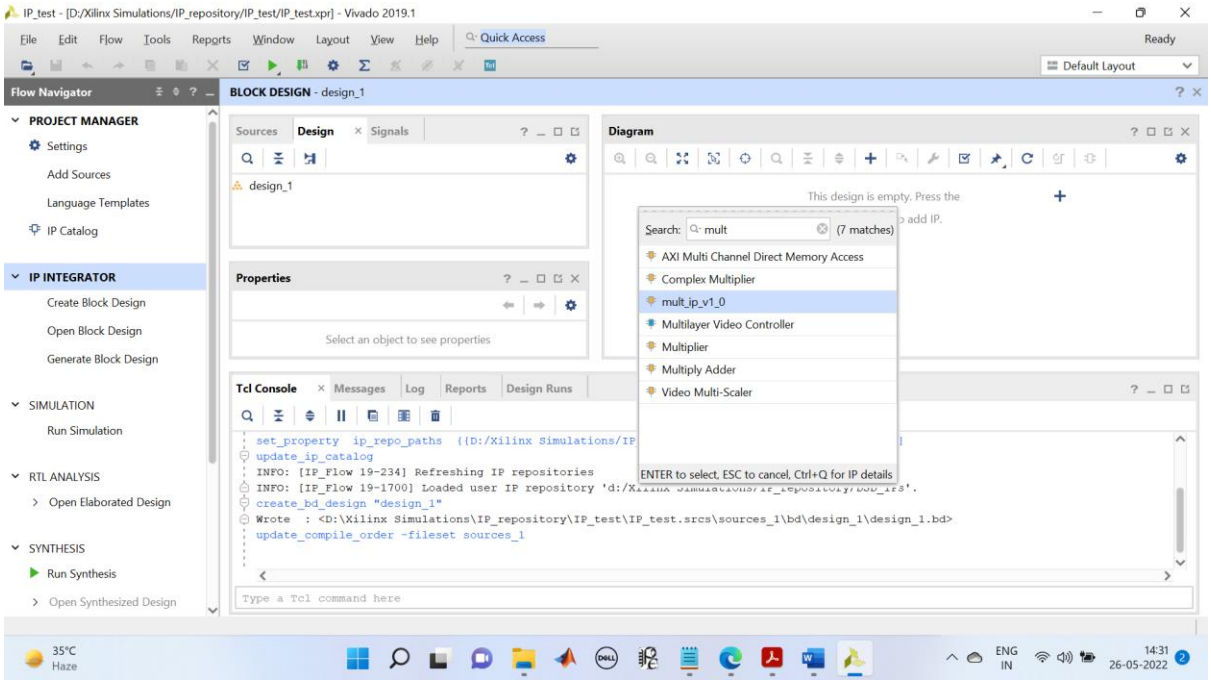


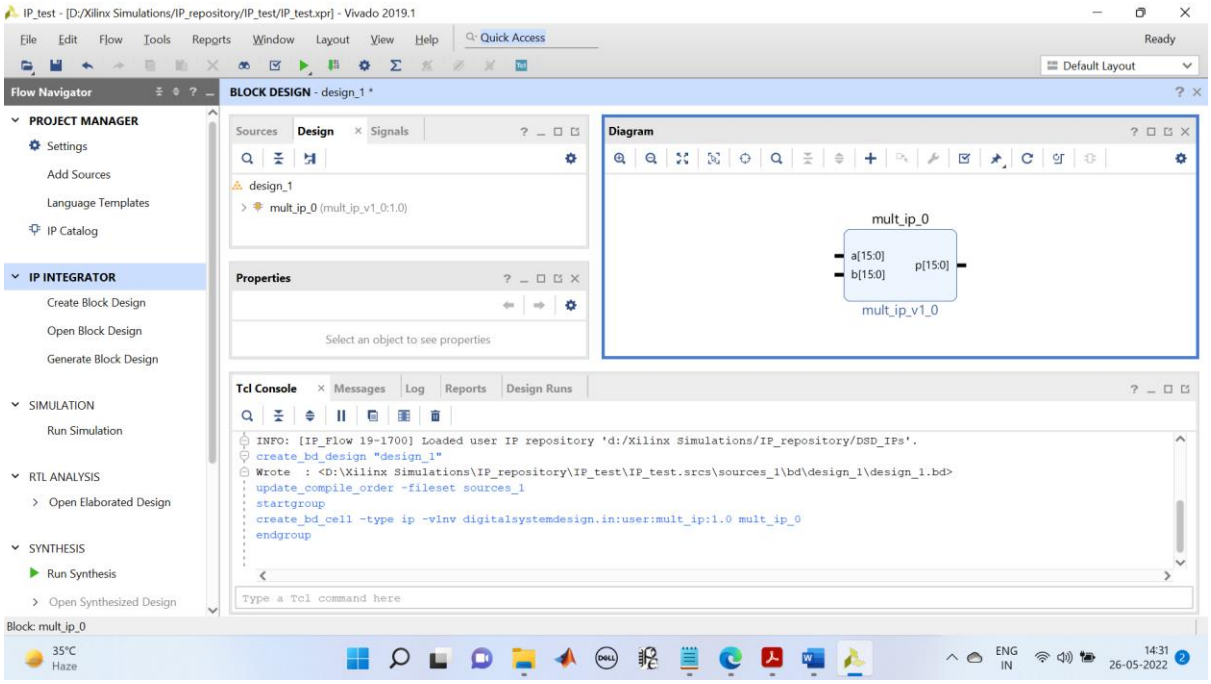
5. Create a block design where the IP will be called.



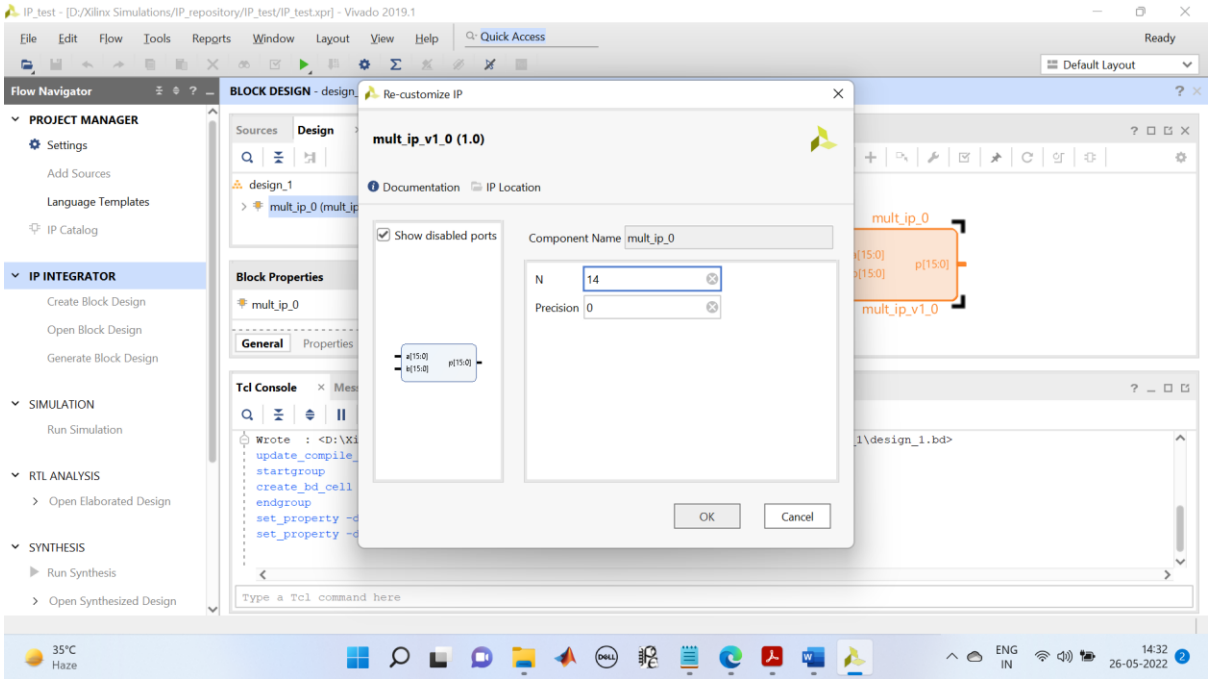


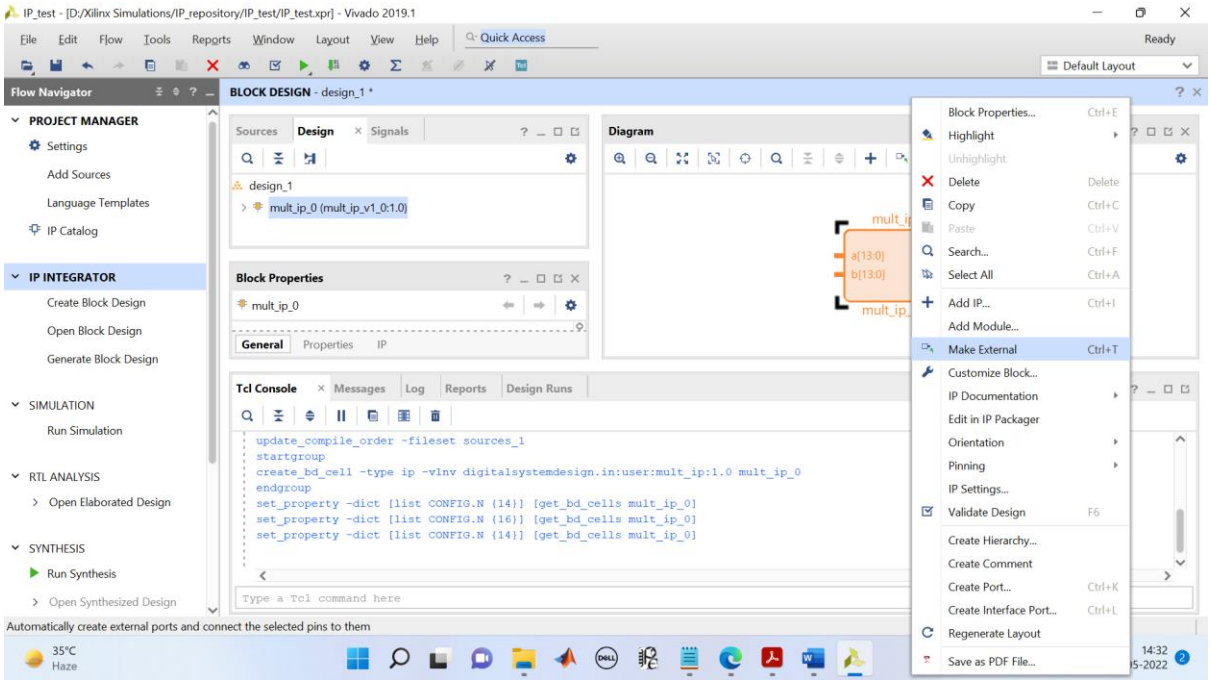
6. By clicking on the Plus symbol all type of IPs can be used. Here use the mult_ip by pressing enter.



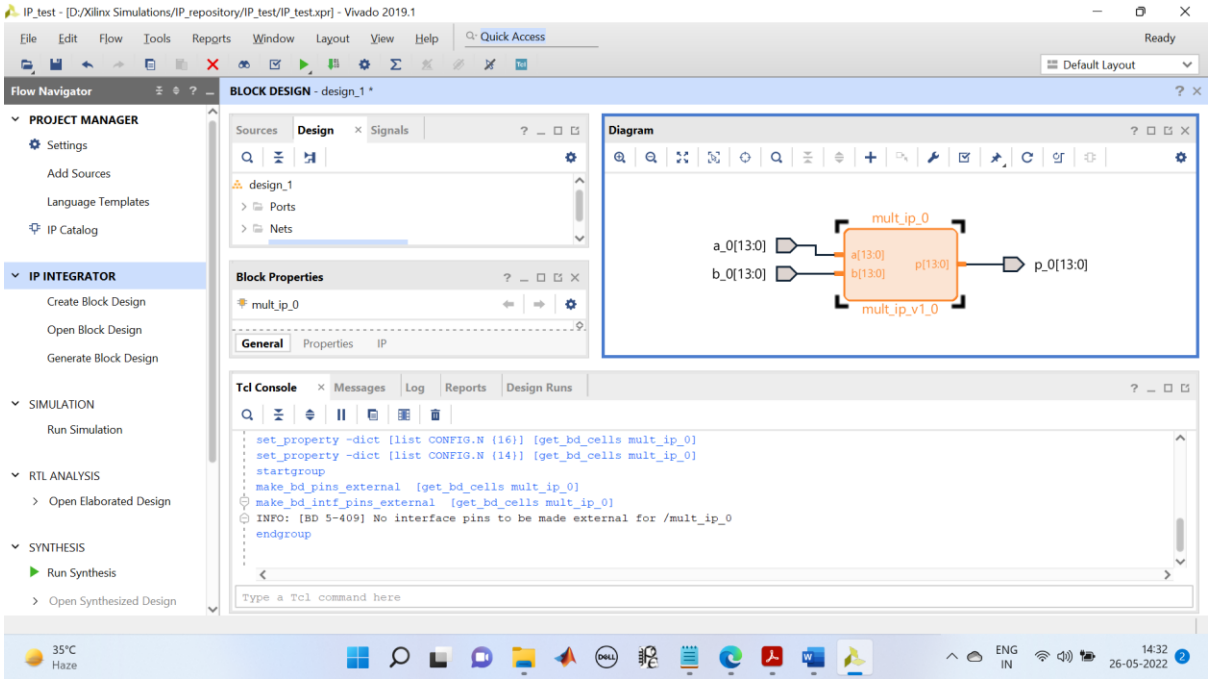


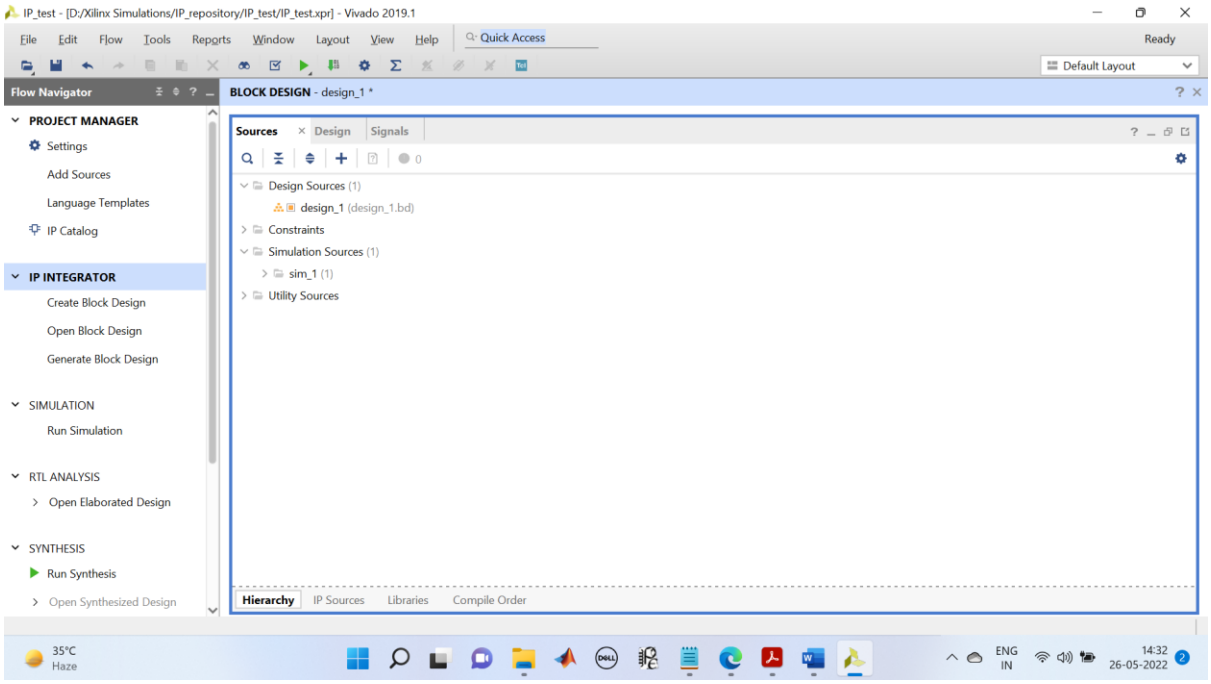
7. Double click on the IP and then a window will pop-up. Here parameters can be changed.



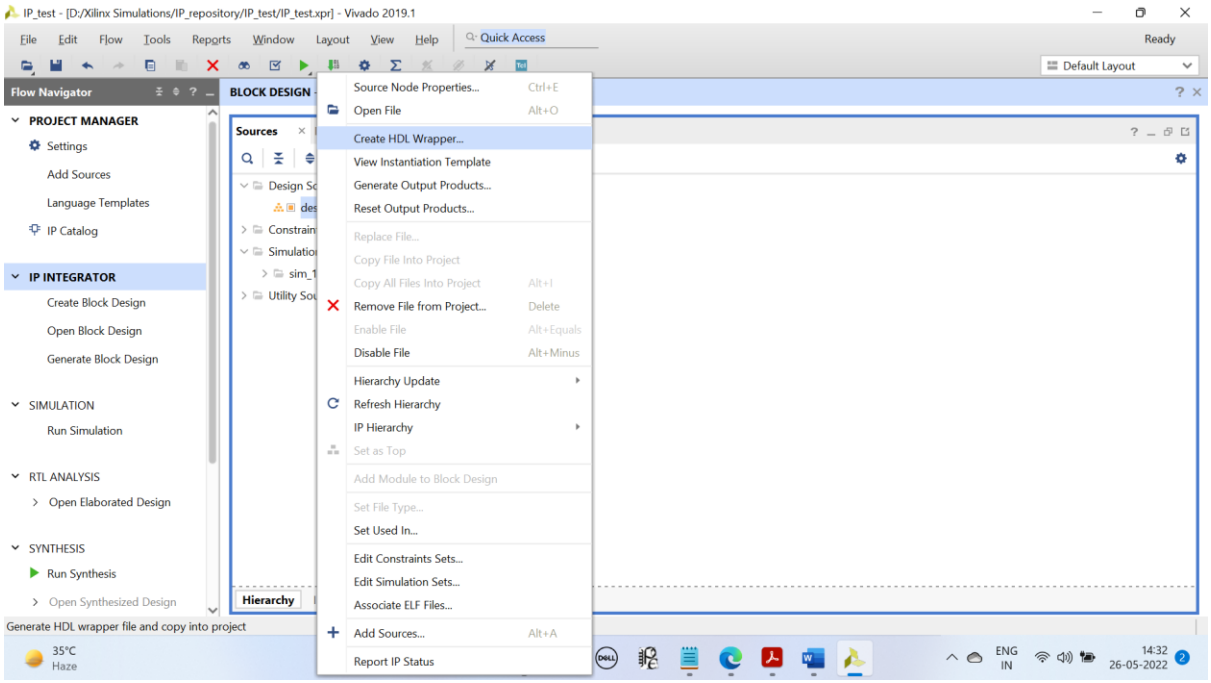


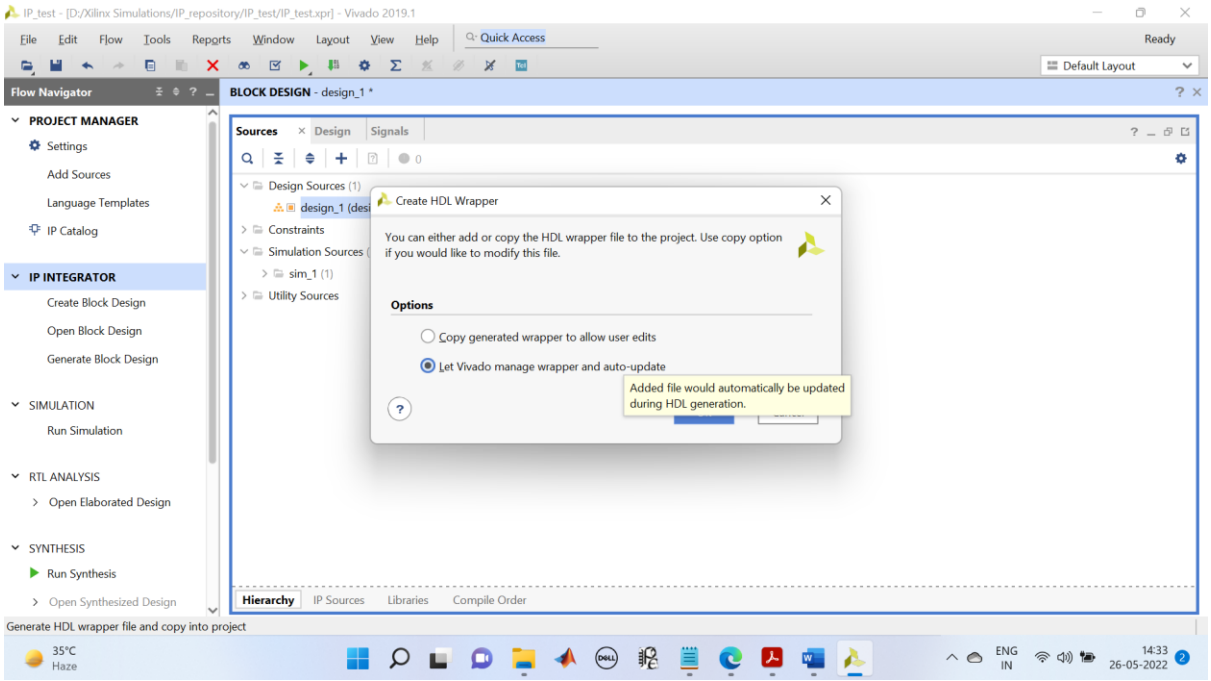
8. By clicking on the IP external connections can be done.





9. Create wrapper Verilog wrapper file of the block design. Without creating wrapper file block design can not be used in the Verilog files.




IP_test - [D:/Xilinx Simulations/IP_repository/IP_test/IP_test.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
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SIMULATION
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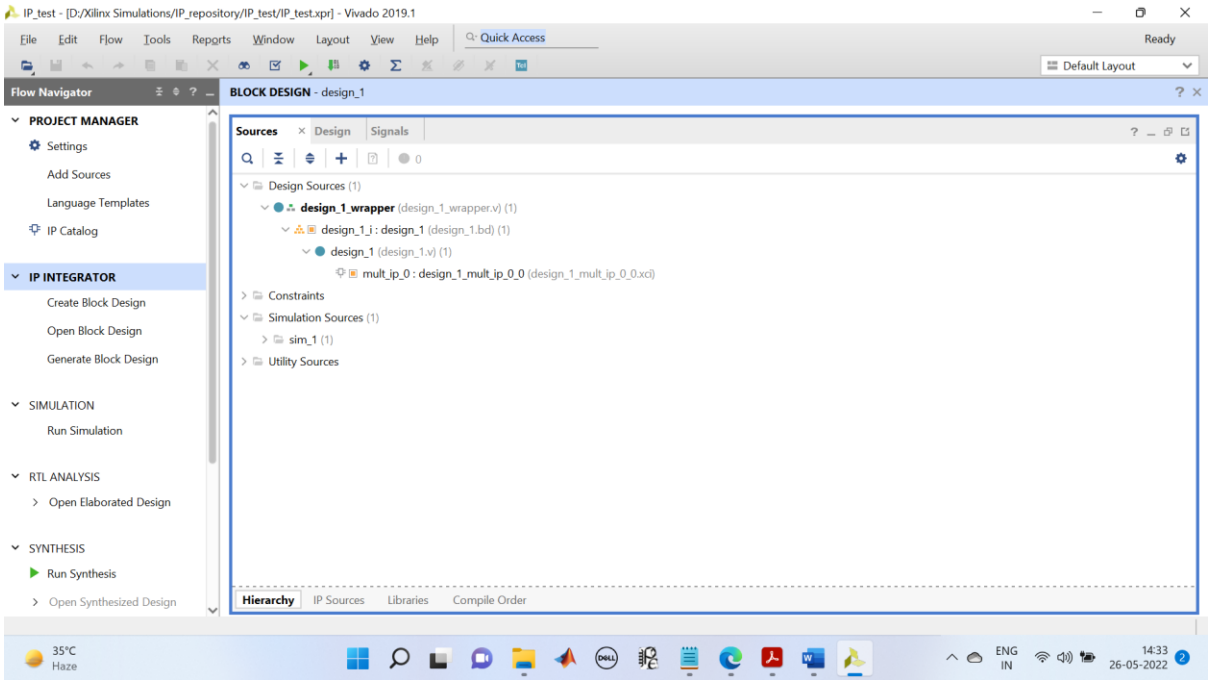
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
BLOCK DESIGN - design_1 *
Sources
Design
Signals
Design Sources (1)
design_1 (desi
Constraints
Simulation Sources
sim_1 (1)
Utility Sources
Create HDL Wrapper
You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.
Options
Copy generated wrapper to allow user edits
Let Vivado manage wrapper and auto-update
Added file would automatically be updated during HDL generation.
Hierarchy
IP Sources
Libraries
Compile Order
Generate HDL wrapper file and copy into project
35°C
Haze
ENG
IN
14:33
26-05-2022


IP_test - [D:/Xilinx Simulations/IP_repository/IP_test/IP_test.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
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Default Layout
Flow Navigator
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Create Block Design
Open Block Design
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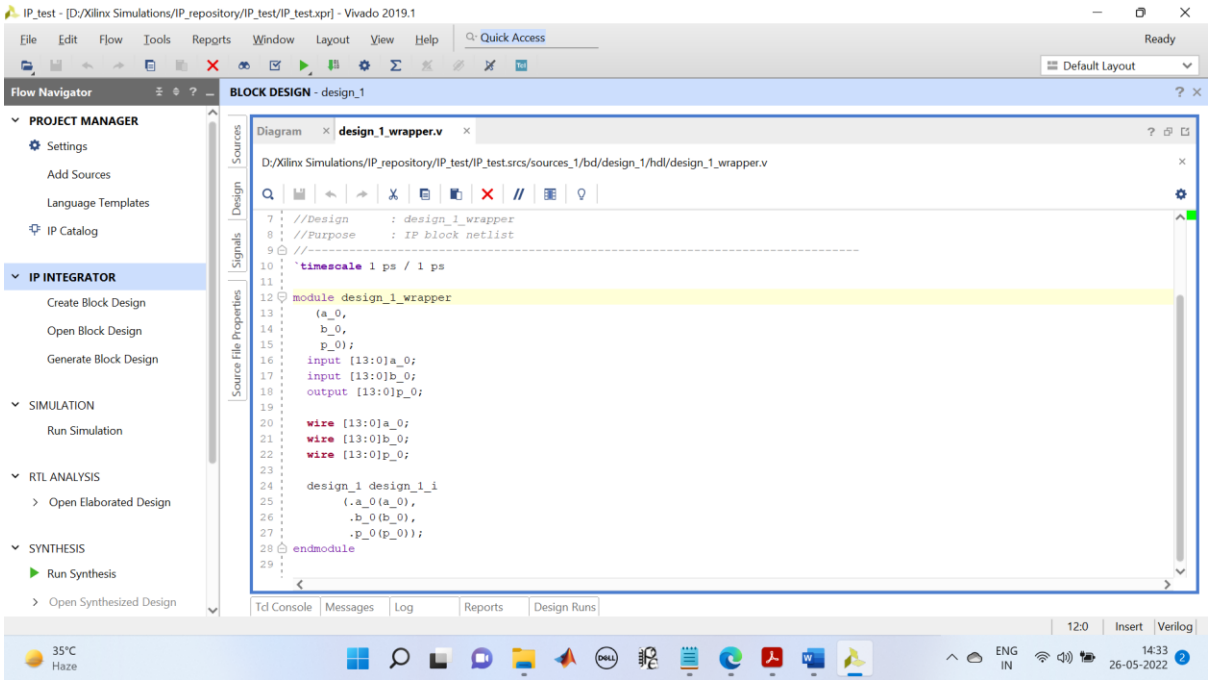
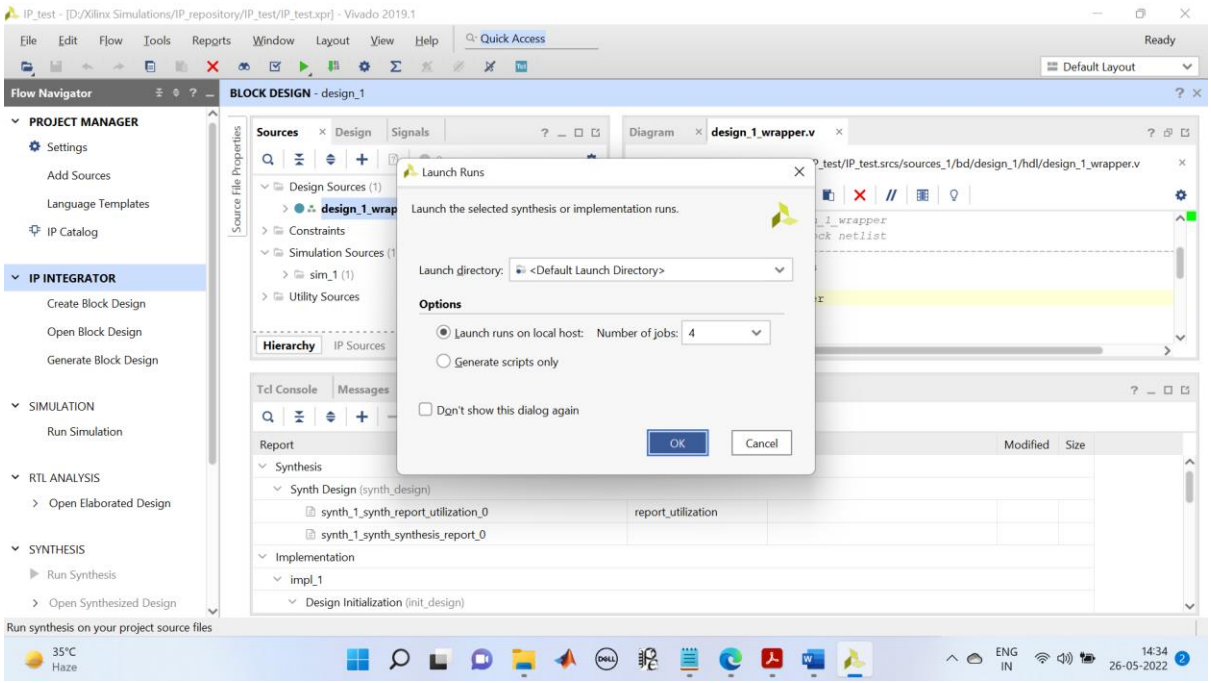
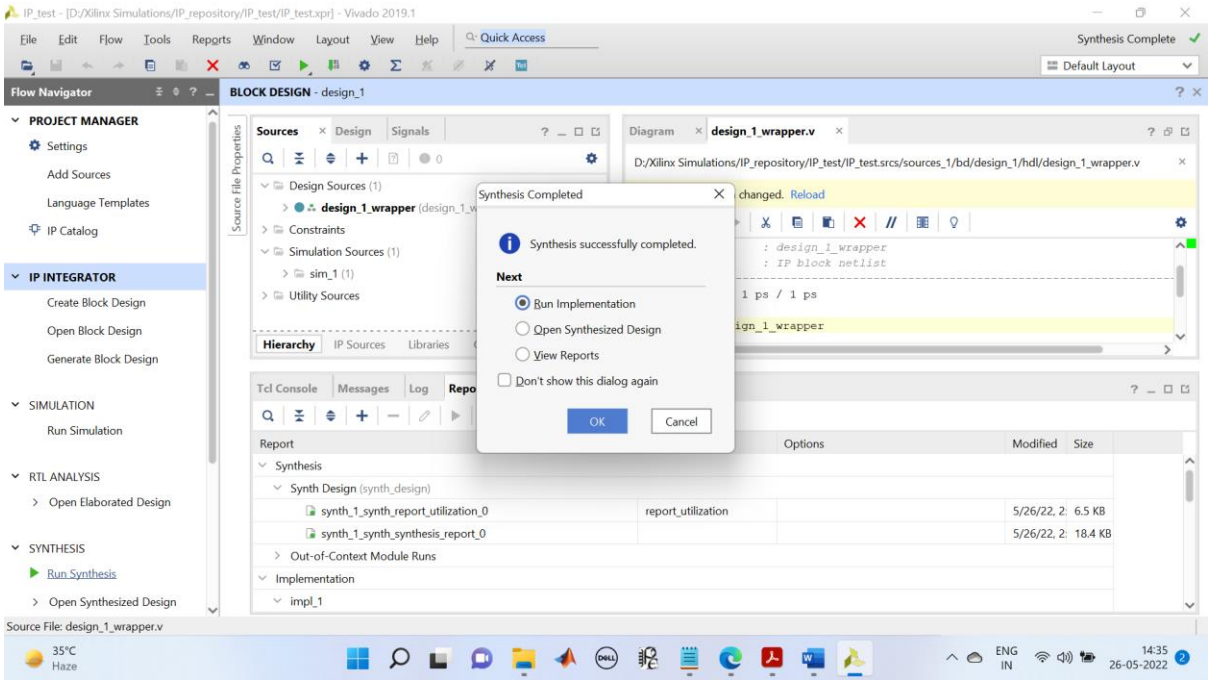
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
BLOCK DESIGN - design_1
Sources
Design
Signals
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
design_1_i : design_1 (design_1.bd) (1)
design_1 (design_1.v) (1)
mult_ip_0 : design_1_mult_ip_0_0 (design_1_mult_ip_0_0.xci)
Constraints
Simulation Sources (1)
sim_1 (1)
Utility Sources
Hierarchy
IP Sources
Libraries
Compile Order
35°C
Haze
ENG
IN
14:33
26-05-2022

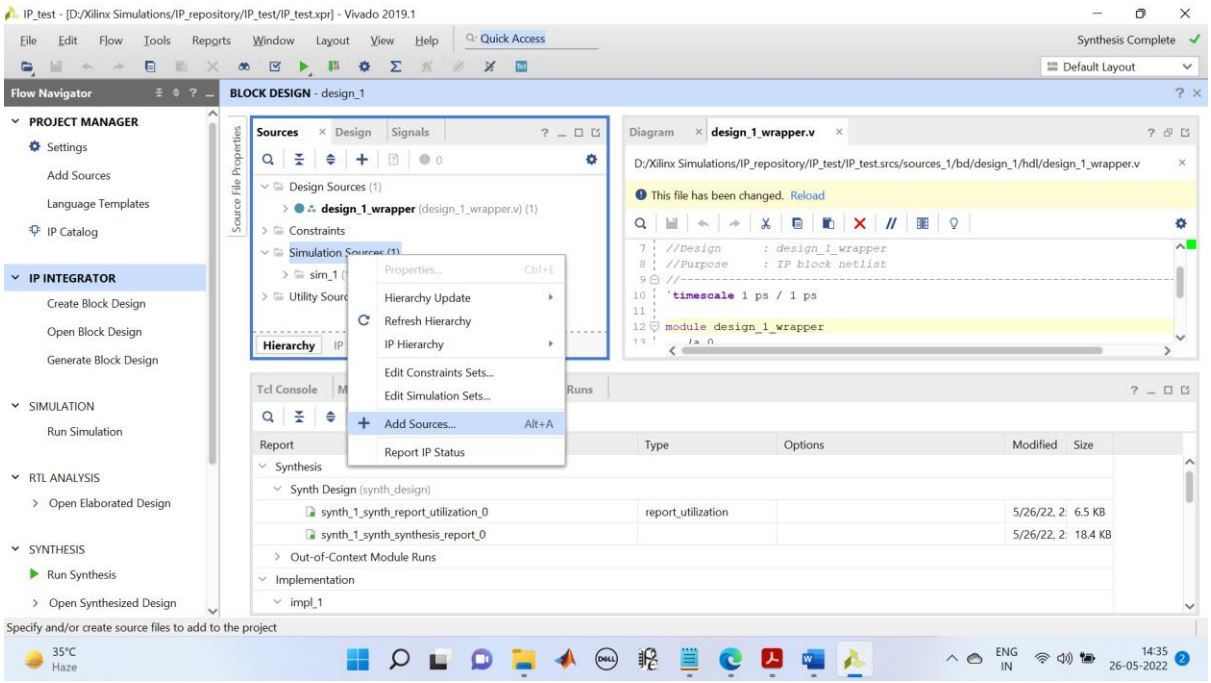


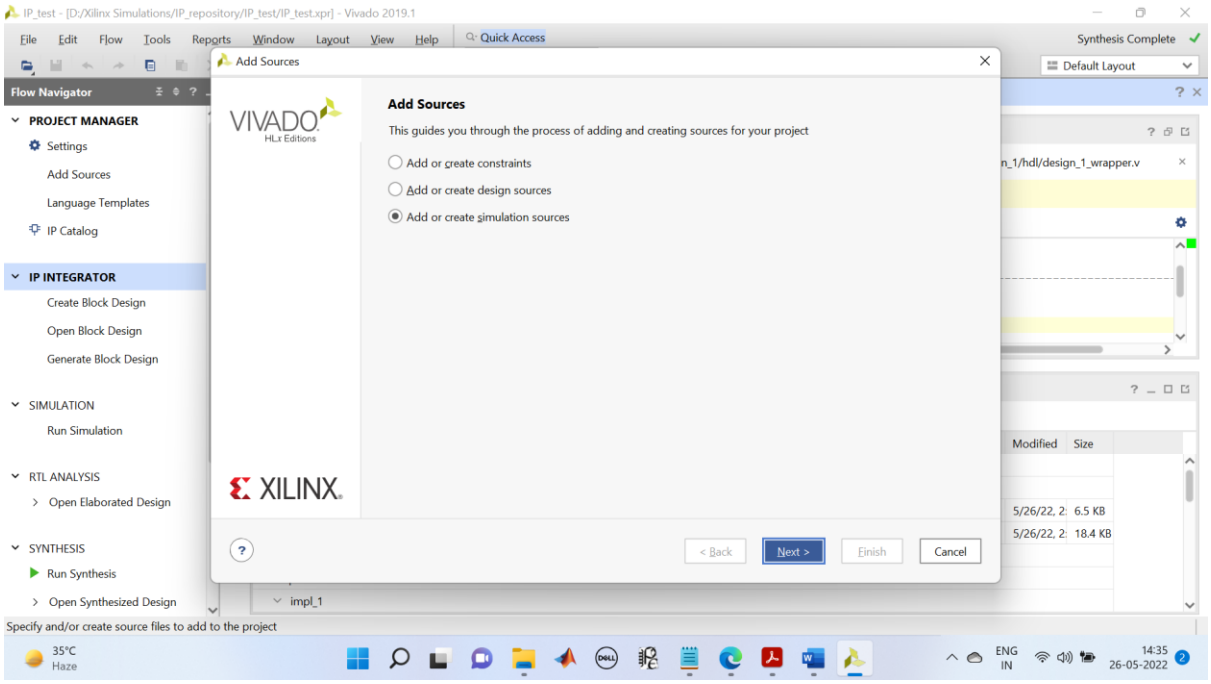
10. Our IP is now instantiated. Now it can be synthesized or Implemented.





11. For simulation we need to write the test bench file.




IP_test - [D:/Xilinx Simulations/IP_repository/IP_test/IP_test.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
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Default Layout
Flow Navigator
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IP Catalog
IP INTEGRATOR
Create Block Design
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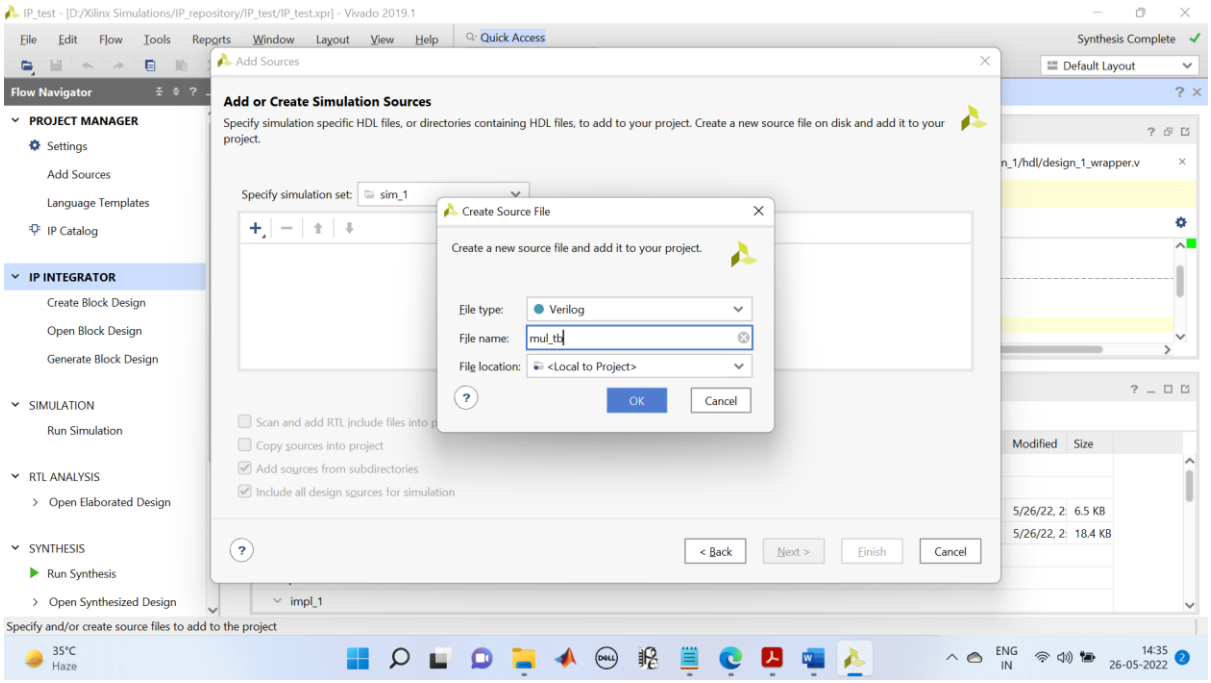
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Add Sources
VIVADO HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel
impl_1
Modified
Size
5/26/22, 2: 6.5 KB
5/26/22, 2: 18.4 KB
Specify and/or create source files to add to the project
35°C
Haze
ENG
IN
14:35
26-05-2022


IP_test - [D:/Xilinx Simulations/IP_repository/IP_test/IP_test.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
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Default Layout
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SIMULATION
Run Simulation
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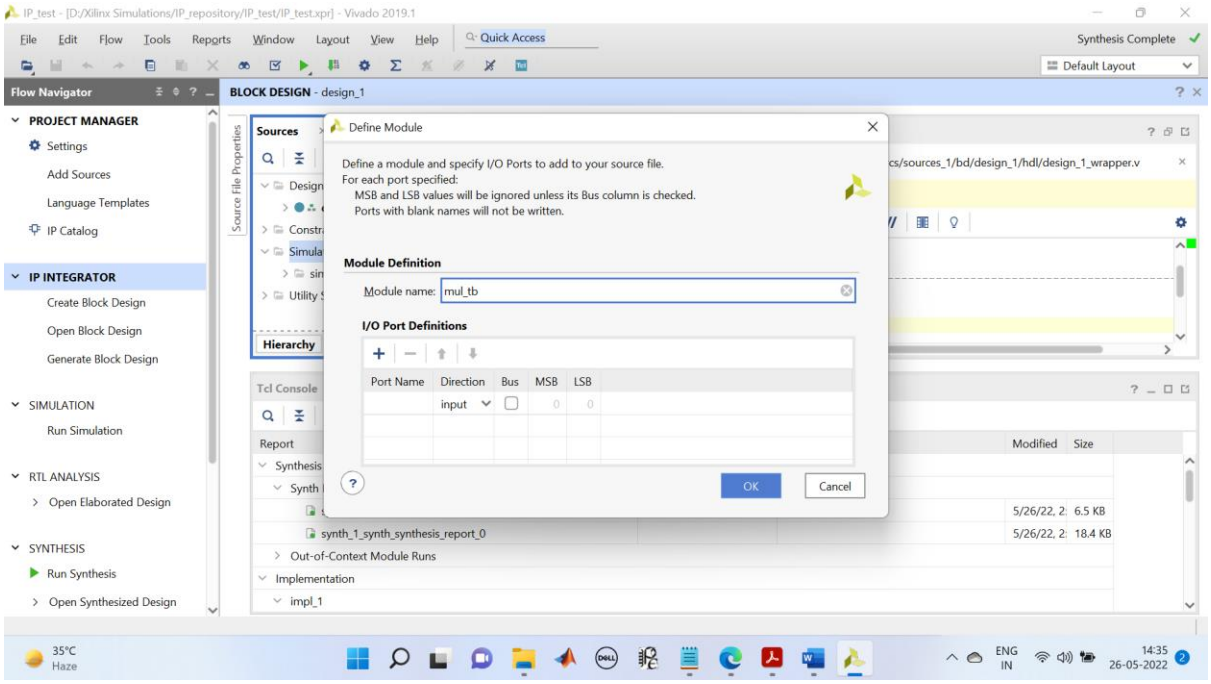
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Create Source File
Create a new source file and add it to your project.
File type:
Verilog
File name:
mul_tb
File location:
<Local to Project>
OK
Cancel
Scan and add RTL include files into p
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel
impl_1
Modified
Size
5/26/22, 2: 6.5 KB
5/26/22, 2: 18.4 KB
Specify and/or create source files to add to the project
35°C
Haze
ENG
IN
14:35
26-05-2022


IP_test - [D:/Xilinx Simulations/IP_repository/IP_test/IP_test.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Default Layout
Flow Navigator
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Generate Block Design
SIMULATION
Run Simulation
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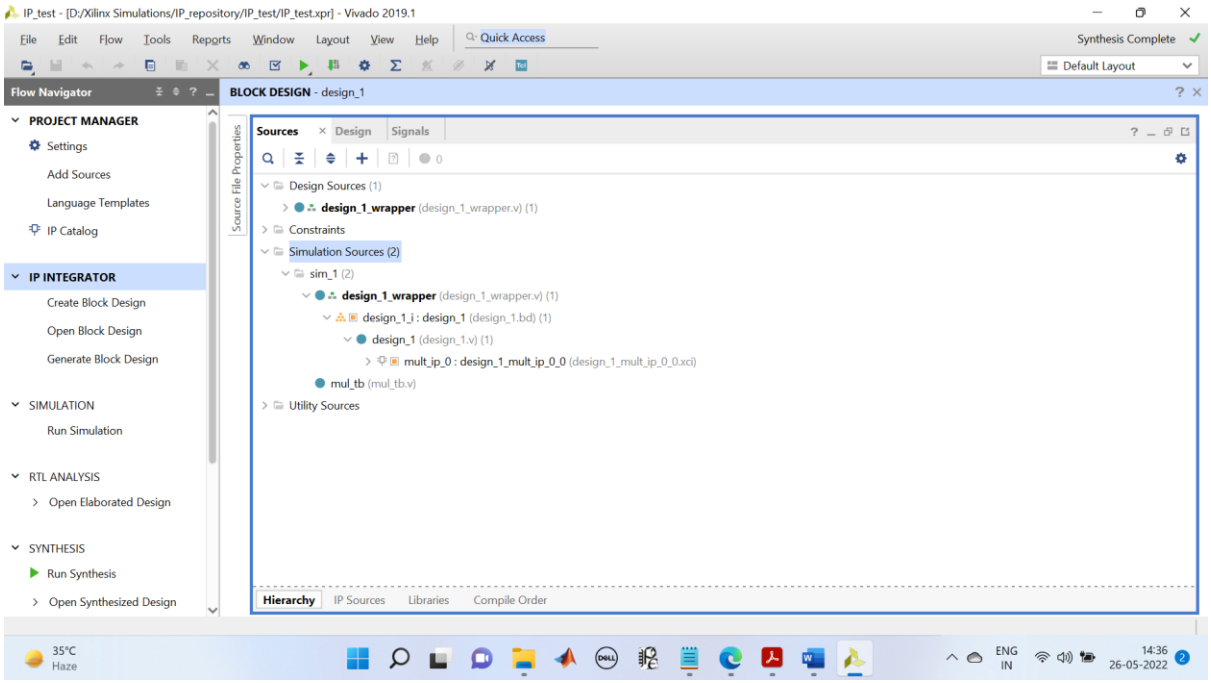
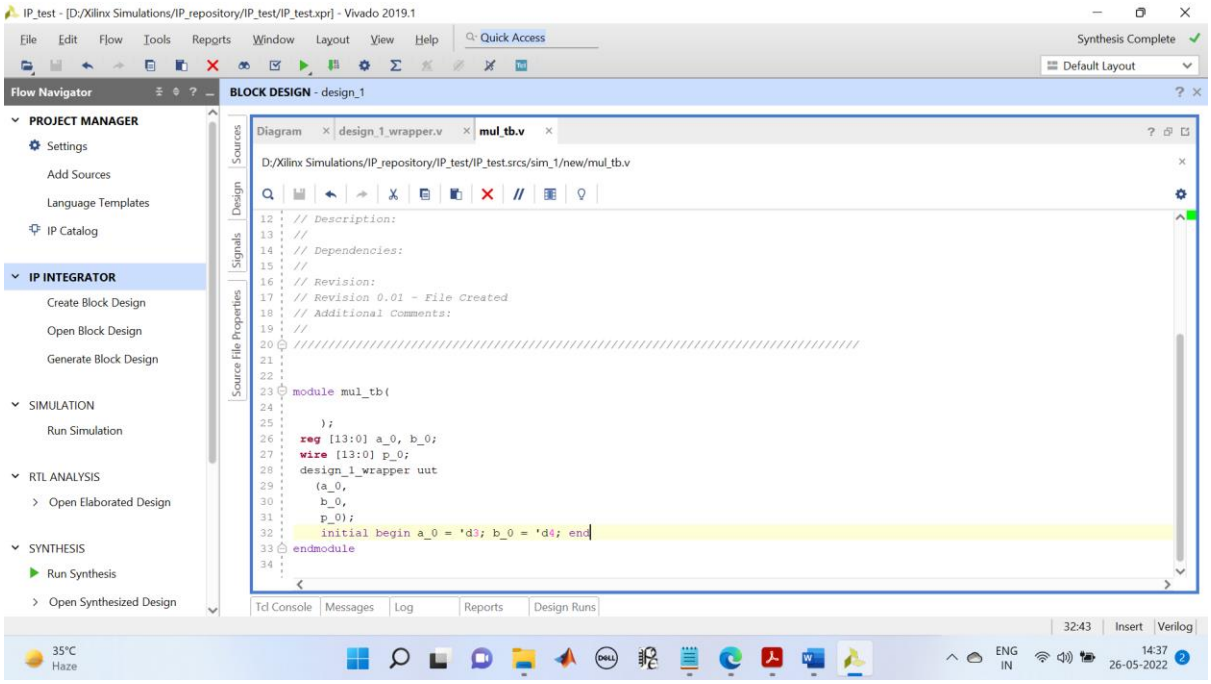
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
BLOCK DESIGN - design_1
Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name: mul_tb
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
input
OK
Cancel
Sources
Hierarchy
Tcl Console
Report
Synthesis
synth_1_synth_synthesis_report_0
Out-of-Context Module Runs
Implementation
impl_1
Modified
Size
5/26/22, 2: 6.5 KB
5/26/22, 2: 18.4 KB
35°C
Haze
ENG
IN
14:35
26-05-2022


IP_test - [D:/Xilinx Simulations/IP_repository/IP_test/IP_test.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
BLOCK DESIGN - design_1
Sources
Design
Signals
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
Constraints
Simulation Sources (2)
sim_1 (2)
design_1_wrapper (design_1_wrapper.v) (1)
design_1_i : design_1 (design_1.bd) (1)
design_1 (design_1.v) (1)
mult_ip_0 : design_1_mult_ip_0_0 (design_1_mult_ip_0_0.xci)
mul_tb (mul_tb.v)
Utility Sources
Hierarchy
IP Sources
Libraries
Compile Order
35°C
Haze
ENG
IN
14:36
26-05-2022


IP_test - [D:/Xilinx Simulations/IP_repository/IP_test/IP_test.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
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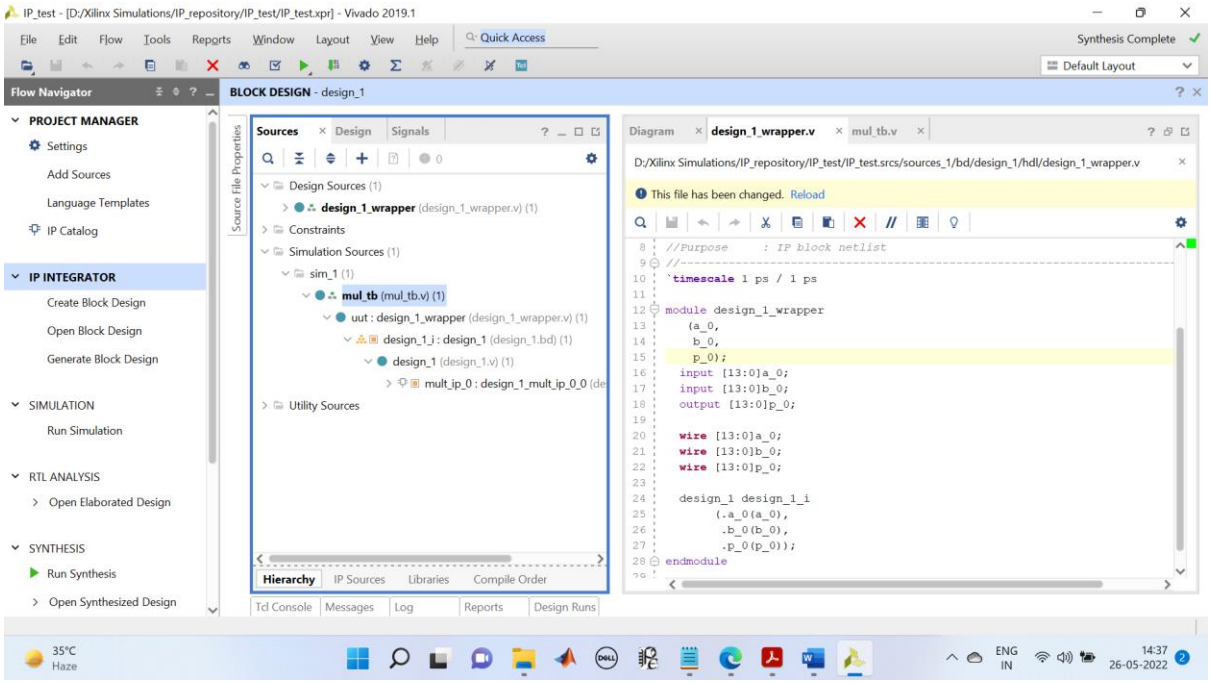
SYNTHESIS
Run Synthesis
Open Synthesized Design
BLOCK DESIGN - design_1
Diagram
design_1_wrapper.v
mul_tb.v
D:/Xilinx Simulations/IP_repository/IP_test/IP_test.srcs/sim_1/new/mul_tb.v
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module mul_tb(
);
reg [13:0] a_0, b_0;
wire [13:0] p_0;
design_1_wrapper uut
(a_0,
b_0,
p_0);
initial begin a_0 = 'd3; b_0 = 'd4; end
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
32:43
Insert
Verilog
35°C
Haze
ENG
IN
14:37
26-05-2022


IP_test - [D:/Xilinx Simulations/IP_repository/IP_test/IP_test.xpr] - Vivado 2019.1
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Quick Access
Synthesis Complete
Default Layout
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Open Block Design
Generate Block Design
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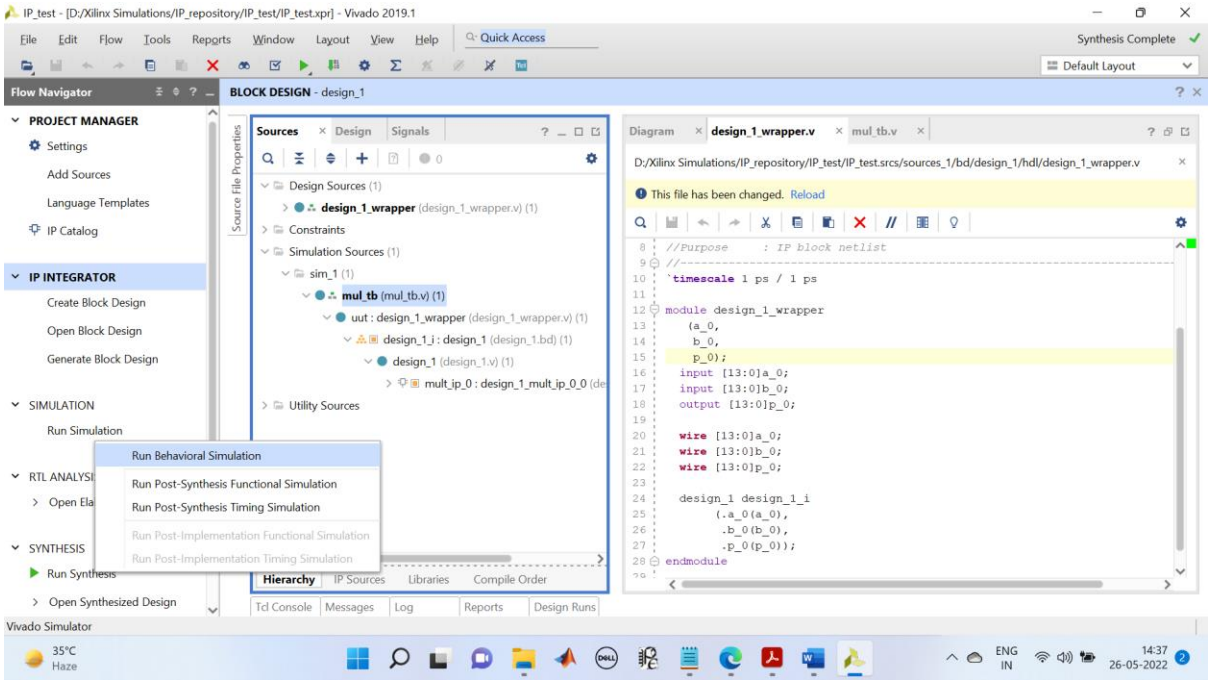
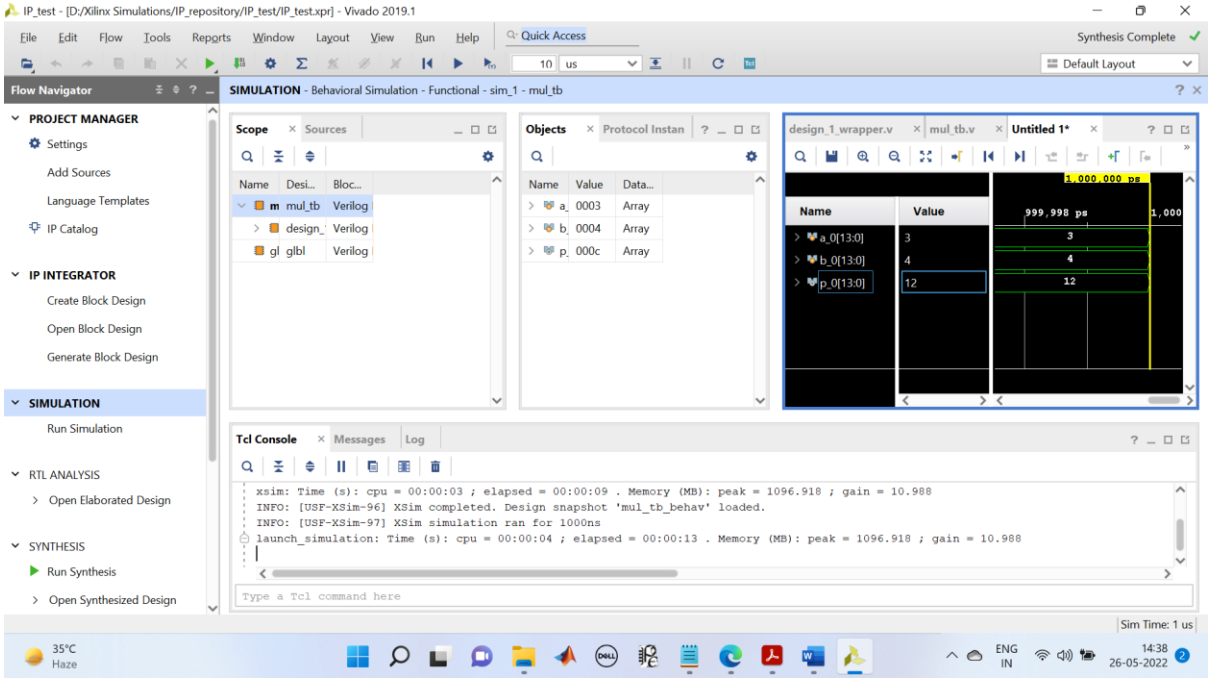
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
BLOCK DESIGN - design_1
Sources
Design
Signals
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
Constraints
Simulation Sources (1)
sim_1 (1)
mul_tb (mul_tb.v) (1)
uut : design_1_wrapper (design_1_wrapper.v) (1)
design_1_i : design_1 (design_1.bd) (1)
design_1 (design_1.v) (1)
mult_ip_0 : design_1_mult_ip_0_0
Utility Sources
Hierarchy
IP Sources
Libraries
Compile Order
Diagram
design_1_wrapper.v
mul_tb.v
D:/Xilinx Simulations/IP_repository/IP_test.srcs/sources_1/bd/design_1/hdl/design_1_wrapper.v
This file has been changed. Reload
//Purpose : IP block netlist
//
`timescale 1 ps / 1 ps
module design_1_wrapper
(a_0,
b_0,
p_0);
input [13:0]a_0;
input [13:0]b_0;
output [13:0]p_0;
wire [13:0]a_0;
wire [13:0]b_0;
wire [13:0]p_0;
design_1 design_1_i
(.a_0(a_0),
.b_0(b_0),
.p_0(p_0));
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
35°C
Haze
ENG
IN
14:37
26-05-2022





Some times problems may arise in Simulation of the designs which uses custom IPs…

To solve that…Few options can be tried.

1. ***Close XILINX and again open it.***
2. ***Replace the IP files with originals ones***
3. ***Select the Block and right click ---First click on ---Reset Output Products***
   Then click on – Generate Output Products
4. ***In the synthesis settings, -flatten_hierarchy---select none and apply first then again select rebuilt.***
5. ***This IP is created using the XILINX Vivado tool 2019.1 and thus it may not be functionally simulated by other tools. Thus, Post Synthesis Functional simulation can be done.***