Digital System Design

We gather, we share, you learn.....

About Us

Digital System Design is a subset of VLSI design. A system on the chip (SoC) is preferred over a system with discrete components mainly because of two constraints viz. speed and area. Nowadays systems, whether they are analog or digital, are implemented to fit on a single chip. A digital system can be a microprocessor/microcontroller, a network system, a communication system, or any implementation of image processing/signal processing algorithms.

In the era of highly developed VLSI design, the demand for the SoCs is growing fast in every field like industrial sectors, communication hubs, etc. The defense sectors are also finding it as a reliable solution to their slow and highly-priced old systems. Researchers are working hard to design systems for a specific task or for a specific application to achieve high speed.

Digital System Design (DSD) LAB is a growing organization which aims to be one of the global leaders in the field of FPGA based system design. It targets to develop efficient Verilog HDL based implementations of digital systems in the field like IoT, Medical, Aerospace or Defense. It also targets to provide good training to students or researchers so that a bright student can be turned into a professional VLSI engineer.

Training Plus Internship Programme

Title: **Training Plus Internship Programme in Design and Implementation of Digital Systems on FPGA using HDL.**

Essential Requirement: **The candidate must satisfy the following criteria,**

1. Candidates must have basic knowledge of Verilog HDL and XILINX EDA tools.
2. Candidates should know the basics of Digital Logic Design/Digital System Design.
3. Candidates having basic Knowledge of FPGA will have an advantage.
4. Candidates must have some knowledge in any of the fields like signal processing, image processing, video processing, or machine learning.
5. Candidates should know the basics of MATLAB and the Simulink tool.

Academic Qualification: **Any Graduation/ Post Graduation/PhD (Pursuing or Completed).**

Problem Statement: **The candidate will be gone through a training session of 6 weeks and after this training session the candidate will be involved in some project implementation. Each candidate will be assigned a problem statement and he/she has to complete the project.**

Internship Benefits: **The following benefits a candidate earns from this internship.**

1. Internship Certificate.

2. Complete guidance to complete the project work.

3. Dissemination of the project work will be published by Digital System Design.

Terms and Conditions:

1. The certificate for the internship will be issued only when the candidate successfully completes the project work.

2. Candidates need to submit a detailed project report with all the source codes.

Notes: **Interested candidates should send their resume to career@digitalsystemdesign.in to apply for the above mentioned training plus internship programme.**

Course Curriculum

All the applicants will become a part of the Internship Program.

The training program has three Stages:

Stage1: Design and Simulation of Digital Systems (DSD)

Duration: 4 Weeks. Location: Virtual

Post completion of 4 weeks the intern will learn the basics of Digital System Design using Verilog. Contents of Stage 1 are

- **Digital System Basics - Basic Combinational and Sequential Circuits**
- **Functional Simulation of these blocks using Verilog.**
- **Memory Design using Verilog.**
- **Finite State Machine Design.**

Stage 2: Classroom Training Program (CRT)

Duration: 2 Weeks. Location: At office location (in person)

Post completion of 2 weeks the intern will be able to implement any design on FPGA. Stage 2 includes

- **FPGA Implementation of Basic Digital Circuits**
- **Interfacing External Devices with FPGA**

Stage 3: Project Training Program (PRT)

Duration: 2 Weeks. Location: Both online and offline mode

Post completion of 2 weeks the intern will be able to implement any project on their own. The content of Stage 3 is

- **Project Implementation**

The training program will be for 2 days a week. The assessment parameters will include performance metrics, capability and quality, and feedback from the supervisor/ trainer. Upon successfully completing the internship program, candidates will become eligible to collect the internship Certificate.

Course Fee: INR 5,000/– for the entire internship program (6+2 weeks).