DIGITAL SYSTEM DESIGN

Website: www.digitalsystemdesign.in

Advt. No: AD001/DSD/1121 **Dated:** 04.11.2021

Job title: Internship on Design and Implementation of a Digital System on FPGA using HDL.

Essential Qualification: BE/BTECH/ME/MTECH in ECE.

Fellowship: No fellowship will be awarded.

Mode of Work: Work from Home (Progress to be monitored through Google Meet).

Problem Statement: Candidate will be involved in a mini-project and the problem statement of the project will be selected based on his/her area of interest. The candidate must finish his/her project during the internship period.

Essential requirement: Candidate must satisfy the following criteria,

1. Candidates must have knowledge of Verilog HDL and XILINX EDA tool. Knowledge of Verilog will be preferred.
2. Candidates should know basics of Digital Logic Design/Digital System Design.
3. Candidates having Knowledge of FPGA implementation will have an advantage.
4. Candidates must have some knowledge in any of the field like signal processing, image processing, video processing or machine learning.
5. Candidates should know basics of MATLAB and Simulink tool.

Internship Benefits: The following benefits a candidate earn from this internship.

1. Internship Certificate.
2. Complete guidance to complete the project work.
3. Dissemination of the project work will be published by Digital System Design.

Terms and Conditions:

1. The certificate for internship will be issued only when the candidate successfully completes the project work.
2. Candidates need to submit a detailed project report with all the source codes.

Notes: Interested candidates should send their recent updated bio-data (Resume) on or before 15th November to **career@digitalsystemdesign.in**.

Selection Process: An initial scrutiny process will be performed to reduce the number of candidates. After the initial scrutiny process an interview will be conducted to select fewer numbers of deserved candidates through Google Meet.