

Curriculum Vitae

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Personal Information

- Name : Ardhendu Sarkar
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- Nationality : Indian
- Gender : Male
- Marital Status : Single
- Spoken Languages : English, Bengali (mother tongue), Hindi
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Present Position:

Junior Research Fellow, Department of Computer Science & Technology,
Indian Institute of Engineering Science & Technology- Shibpur Howrah-711103, India
• **Thesis Supervisor:** Prof. Surajeet Ghosh

Academic Qualifications

PhD in *Computer Science & Technology* (2018- Present)
Department of Computer Science & Technology
Indian Institute of Engineering Science &
Technology- Shibpur Howrah-711103

MTech in *Information Technology s* (2014-16)
Department of Information Technology
Indian Institute of Engineering Science & Technology- Shibpur Howrah-711103

BTech with *Computer Science & Technology* (2008-12)
Govt. College of Engg. & Textile Technology, Berhampore- 742101 (Affiliated to Maulana Abul Kalam Azad University of Technology), West Bengal, India
Division/Class: 1st

10+2 with *Physics, Chemistry, Mathematics, Biology, English and Bengali* (2007)
West Bengal Council of Higher Secondary Education, India
Division/Class: 1st

10-th standard with Physical science, Life Science, Mathematics, English and Bengali (2005)
West Bengal Board of Secondary Education, India
Division/Class: 1st

List of Publications

1. A. Sarkar, S. Banerjee and S. Ghosh, "An Energy-Efficient Pipelined-Multiprocessor Architecture for Biological Sequence Alignment," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, doi: 10.1109/TVLSI.2020.3015138.

Conference and Workshop

- A. Sarkar and S. Ghosh, "A Coarse-Grained Pipeline Architecture for Sequence Alignment," 2018 15th IEEE India Council International Conference (INDICON), Coimbatore, India, 2018, pp. 1-6, doi: 10.1109/INDICON45594.2018.8987014.
- A. Sarkar, K. Ray, D. Chowdhury, K. Sahu, S. Kundu and S. Ghosh, "Time and Space Efficient Optimal Pairwise Sequence Alignment using GPU," TENCON 2019 - 2019 IEEE Region 10 Conference (TENCON), Kochi, India, 2019, pp. 423-428, doi: 10.1109/TENCON.2019.8929482.
- "Workshop on FPGA Based Digital System Design" from 15th Jan. to 19th Jan. 2018, Dept. of CST, IEST, Shibpur.

References

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Declaration:

I hereby declare that the details stated above are true and correct to the best of my knowledge.